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Docket No.: 08211/0200253-US0/P05742
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Timothy L. Blankenship, et al.

Application No.: 10/724,028 Confirmation No.: 7271

Filed: November 26, 2003

For: APPARATUS FOR CIRCUIT WITH KEEPER

PETITION UNDER 37 CFR 1.47(a) REGARDING NON-SIGNING INVENTOR

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 CFR § 1.47(a), it is respectfully requested that the above-identified patent application be accepted as complete with a partially executed Combined Declaration and Power of Attorney, which has been signed by one of the two inventors, Timothy L. Blankenship. The non-signing inventor, Sijian Chen, has refused to cooperate and sign both the Combined Declaration and Power of Attorney and Assignment regarding his inventorship of the above-identified patent application as required to do under the terms of his previous employment with the assignee.

Filed with this petition is a Declaration under 37 CFR § 1.47(a), which provides the pertinent facts regarding Sijian Chen's refusal to sign the Combined Declaration and Power of Attorney document.

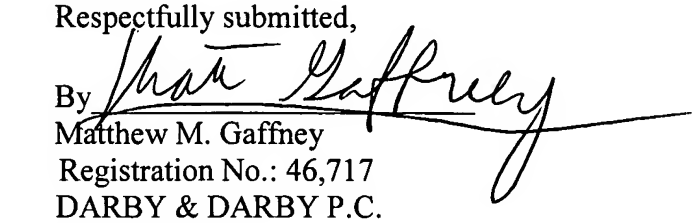
Also filed with this petition is the original Combined Declaration and Power of Attorney documents signed by one of the two inventors.

Sijian Chen's last known address is 12504 Edward Hollow Run, Austin, Texas 78739.

A check in the amount of $130.00 is enclosed to cover the petition fee as required by 37 CFR § 1.17(h).

Dated: June 25, 2004

Respectfully submitted,

By 

Matthew M. Gaffney
Registration No.: 46,717
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257
(206) 262.8900
(212) 753-6237 (Fax)
Attorneys/Agents For Applicant

Docket No.: 08211/0200253-US0/P05742
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Timothy L. Blankenship, et al.

Application No.: 10/724,028 Confirmation No.: 7271

Filed: November 26, 2003

For: APPARATUS FOR CIRCUIT WITH KEEPER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

DECLARATION UNDER 37 CFR 1.47(a) REGARDING NON-SIGNING INVENTOR

TABLE OF CONTENTS

Declaration Under 37 CFR 1.47(a) Regarding Non-Signing Inventor

Copy of 03/26/04 Email to Sijian Chen regarding Combined Declaration and Power of Attorney and Assignment for signature. Exhibit 4

Copy of 03/28/04 Email from Sijian Chen regarding Combined Declaration and Power of Attorney and Assignment for signature. Stating "I was let go by National at a difficult time of my life when I just had a new child and my wife was still sick at home. As much as I'd like to help National out completing the patent applications, I have many other obligations that's at higher priority. I'm afraid I do not have any time at the present to review the papers. Please remove my e-mail address and contact information from your contact list". Exhibit 5

Copy of 03/29/04 Email to Sijian Chen regarding Combined Declaration and Power of Attorney and Assignment for signature. Exhibit 6

Copy of Letter and Enclosures sent to Sijian Chen via Federal Express on 04/20/04. Exhibit 7

Copy of returned package from Federal Express stating "Recipient Not at This Address". Dated 04/21/04. Exhibit 8

Copy of email sent 04/21/04 containing a voicemail from Federal Express stating "Recipient Not at This Address" Exhibit 9

Copy of 04/25/04 Email to Sijian Chen regarding Combined Declaration and Power of Attorney and Assignment for signature. Exhibit 10

Copy of Letter and Enclosures sent to Sijian Chen via Federal Express on 04/27/04. Exhibit 11

Copy of Federal Express website printout stating that delivery was attempted and the customer was not available or business closed. Exhibit 12

I, Matthew M. Gaffney, declare that:

1. I am an attorney of the State of Washington given recognition pursuant to 37 CFR § 10.6 to prepare and prosecute patent applications before the United States Patent and Trademark Office.

2. I represent National Semiconductor Corporation, of Santa Clara, California, in prosecuting a patent application, entitled APPARATUS FOR CIRCUIT WITH KEEPER, and assigned attorney docket number 08211/0200253-us0/P05742, Serial Number 10/724,028, filed November 26, 2003.

3. I have personal knowledge of the matters set forth herein.

4. I am over the age of majority and am competent to be a witness in this matter.

5. On November 20, 2003, I caused to be emailed to Sijian Chen an Assignment and Combined Declaration and Power of Attorney. A copy of this email is Attached hereto. See Exhibit 1.

6. On March 12, 2004, I caused to be emailed to Sijian Chen an Assignment and Combined Declaration and Power of Attorney. A copy of this email is Attached hereto. See Exhibit 2.

7. On March 25, 2004, I caused to be emailed to Sijian Chen an Assignment and Combined Declaration and Power of Attorney. A copy of this email is Attached hereto. See Exhibit 3.

8. On March 26, 2004, I caused to be emailed to Sijian Chen an Assignment and Combined Declaration and Power of Attorney. A copy of this email is Attached hereto. See Exhibit 4.

9. On March 28, 2004, I was contacted via email by Sijian Chen regarding the Assignment and Combined Declaration and Power of Attorney. A copy of this email is Attached hereto. See Exhibit 5.

10. On March 29, 2004, I caused to be emailed to Sijian Chen an Assignment and Combined Declaration and Power of Attorney. A copy of this email is Attached hereto. See Exhibit 6.

11. In the cover letter dated April 20, 2004, Sijian Chen was asked to review a copy of the above-identified patent application. If the patent application met with his approval, we asked him to execute the Assignment and Combined Declaration and Power of Attorney documents and return them to us for filing with the U.S. Patent and Trademark Office. See Exhibit 7.

12. On April 21, 2004, I received a return package from Federal Express stating that "Recipient Not at This Address". See Exhibit 8.

13. On April 21, 2004, I received a voicemail message from Federal Express stating that delivery was attempted and "Recipient Not at This Address". See Exhibit 9.

14. On April 25, 2004, I caused to be emailed to Sijian Chen a statement asking for Sijian Chen to either sign the documents, or tell us that he refused. A copy of this email is Attached hereto. See Exhibit 10.

15. In the cover letter dated April 27, 2004, Sijian Chen was asked to review a copy of the above-identified patent application. If the patent application met with his approval, we asked him to execute the Assignment and Combined Declaration and Power of Attorney documents and return them to us for filing with the U.S. Patent and Trademark Office. See Exhibit 11.

16. On April 28, 2004, my assistant checked the Federal Express website and it stated "Recipient Not at This Address". See Exhibit 12

17. Sijian Chen has repeatedly refused to cooperate in the preparation and filing of the above-identified patent application as required to do under the terms of his previous employment with the assignee.

18. Sijian Chen's last known address is:

12504 Edward Hollow Run
Austin, TX 78739

I hereby declare under penalty of perjury under the laws of the United States of America that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the patent application or any patent issued thereon.

Matthew M. Gaffney
Reg. No. 46,717

6/25/04
Date

Livingston, Shannon

From: Livingston, Shannon
Sent: Friday, March 12, 2004 3:50 PM
To: 'tblankenship1@austin.rr.com'
Cc: 'Schen4@austin.rr.com'
Subject: Corrected Formal Papers for 08211/0200253-US0/P05742 and 08211/0200254-US0/P05741

Hello - I have taken over responsibility for the above-referenced cases. I looked at the e-mails between Janice Kniep and yourself. I am forwarding to you the "new" Formal Papers for filing after the application has been filed. If you both could sign, fax back and return by mail as soon as is convenient for you I would greatly appreciate it. Thank you in advance for your time.

Attached please find: 1) an Assignment and 2) a Combined Declaration and Power of Attorney document. Please print the Assignment document (single-sided) and check that the information is correct. If the information is correct, please sign where indicated before a notary. Please print the Combined Declaration and Power of Attorney (single-sided) and also confirm the information is correct in this document. If the information is correct, please sign on the last page . Please return the signed documents by facsimile (fax number 206.262.8901) and by mail to John Branch at Darby & Darby P.C., 1191 Second Avenue, Suite 1900, Seattle, Washington 98101. If there is incorrect information please let me know as soon as possible so we can correct the errors. We have a deadline of April 27, 2004 for filing these documents for "Missing Parts".

Should you have any questions, please do not hesitate to email me.

Dec and POA.pdf
(57 KB)

Assignment.pdf (27
KB)

Dec and POA.pdf
(78 KB)

Assignment.pdf (24
KB)

Sincerely,

Shannon Livingston
Secretary
Darby & Darby P.C.
1191 Second Avenue
Seattle, WA 98101

206.262.8953 | direct

206.262.8901 | fax

http://www.darbylaw.com.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is described and claimed and for which a patent is sought on the invention entitled:

APPARATUS FOR CIRCUIT WITH KEEPER

the specification of which was filed on November 26, 2003 as Application No. 10/724,028.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to herein. I do not know and do not believe that the same was ever known or used in the United States of America before my or our invention thereof or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, or in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigned more than twelve months prior to this application.

I acknowledge the duty to disclose all information known to me that is material to patentability in accordance with Title 37, Code of Federal Regulations, § 1.56.

FOREIGN PRIORITY CLAIM

I hereby claim foreign priority benefits under Title 35, United States Code § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

[x] no such foreign applications have been filed

[ ] such foreign application have been filed as follows:

EARLIEST FOREIGN APPLICATION(S), IF ANY FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION

Application Number	Country	Date of Filing	Priority Claimed Under 35 USC 119
			___ Yes No ___

ALL FOREIGN APPLICATION(S), IF ANY FILED MORE THAN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION

Application Number	Country	Date of Filing

CLAIM FOR BENEFIT OF EARLIER U.S. PROVISIONAL APPLICATIONS

I hereby claim priority benefits under Title 35, United States Code §119(e), of any United States provisional patent application(s) listed below:

[x] no such U.S. provisional applications have been filed.

[ ] such U.S. provisional application have been filed as follows:

Application Number	Date of Filing	Priority Claimed Under 35 USC 119
		___ Yes No ___

CLAIM FOR BENEFIT OF EARLIER U.S./PCT APPLICATION(S)

I hereby claim the benefit under Title 35, United States Code, §120 of the United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose all information that is material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56 which became available to me between the filing date of the prior application and the national or PCT international filing date of this application:

[x] no such U.S./PCT applications have been filed.

[ ] such U.S./PCT application have been filed as follows:

Application Number	Date of Filing	Status (Patented/Pending/Abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made

with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the practitioners under Customer Number

38845

all of **Darby & Darby P.C.**, P.O. Box 5257, New York, New York 10150-5257, jointly, and each of them severally, my attorneys at law/patent agent(s), with full power of substitution, delegation and revocation, to prosecute this application, to make alterations and amendments therein, to receive the patent, and to transact all business in the U. S. Patent and Trademark Office connected therewith.

Please mail all correspondence to John W. Branch, whose address is:

Darby & Darby P.C.
P.O. Box 5257
New York, New York 10150-5257

Please direct telephone calls to: John W. Branch at (206) 262-8900.

Please direct facsimiles to: (212) 753-6237

Full name of sole or first inventor Timothy L. Blankenship	
Sole or first inventor's signature	Date
Residence Austin, Texas	
Citizenship US	
Mailing Address 4613 Saloma Place Austin, Texas 78749	

Full name of second inventor, if any Sijian Chen	
Second inventor's signature	Date
Residence Austin, Texas	
Citizenship China	
Mailing Address 9114-B Sedgemoor Tr. Austin, Texas 78748	

Attorney Docket No.: 08211/0200253-US0

ASSIGNMENT

I, Timothy L. Blankenship, a citizen of US, residing at 4613 Saloma Place; Austin, Texas 78749; and

I, Sijian Chen, a citizen of China, residing at 9114-B Sedgemoor Tr.; Austin, Texas 78748;

and each of us, if more than one person is identified above (hereinafter "ASSIGNOR") in consideration of the sum of Ten Dollars ($10.00), or the equivalent thereof, and other good and valuable consideration, the sufficiency of which and receipt of which are hereby acknowledged, paid to ASSIGNOR by

National Semiconductor Corporation

a Corporation organized under the laws of Delaware, located at 2900 Semiconductor Drive, Santa Clara, California 95051-8090 (hereinafter "ASSIGNEE"), do hereby sell and assign to said ASSIGNEE, its successors and assigns, the below indicated right, title, and interest, **throughout the world** in and to my Invention entitled:

APPARATUS FOR CIRCUIT WITH KEEPER

invented by me and described in Patent Application No. 10/724,028, filed on November 26, 2003, in the United States; and all patents, divisions, reissues, continuations and any extensions thereof and rights of priority therein, said interest being my entire ownership interest in the same, to be held and enjoyed by said ASSIGNEE, its successors, assigns, or other legal representatives, to the full end of the term thereof, as fully and entirely as the same would have been held and enjoyed by me if this assignment and sale had not be made;

And for the consideration aforesaid, I hereby covenant and agree to and with said ASSIGNEE, its successors and assigns, that whenever ASSIGNEE, its counsel or representative, or the counsel or representative of its successors or assigns, shall advise that an amendment to, or

rights associated with the Invention, or for the reissue or continuation or extension of the same, will do all acts necessary or required to secure in said ASSIGNEE, its successors or assigns, the title to and full benefit of all rights hereby assigned, without charge to said ASSIGNEE or its successors or assigns, but at its or their expense; and I hereby appoint every present or future officer of said ASSIGNEE as my agent to sign all such papers and to do all such necessary acts on my behalf, to the fullest extent permitted by law;

And I hereby authorize and request the Commission of Patents and Trademarks and any other granting authority to issue any Letters Patent resulting from said Invention and application(s) concerning same to said ASSIGNEE.

This assignment shall have an effective date corresponding to the last date of execution.

I declare under penalty of perjury under the laws of the United States of America, and under penalty of the laws of any other jurisdiction before which this document may be presented, that I have signed this document as my own free act and that all of the foregoing is true and correct.

IN TESTIMONY WHEREOF, I have hereunto set my hand this _____ day of _____, 2004

_____
Timothy L. Blankenship

STATE OF _____)
)ss.
COUNTY OF _____)

On this _____ day of _____, 2004, before me personally appeared Timothy L. Blankenship to me known and known to me to be the person described in and who executed the foregoing instrument, and he duly acknowledged to me that he executed the same for the uses and purposes therein set forth.

[SEAL]

_____
Notary Public

Livingston, Shannon

From: Livingston, Shannon
Sent: Thursday, March 25, 2004 12:40 PM
To: 'tblankenship1@austin.rr.com'
Cc: 'Schen4@austin.rr.com'
Subject: FW: Corrected Formal Papers for 08211/0200253-US0/P05742 and 08211/0200254-US0/P05741

Hello - Even though it has only been about 2 weeks, I just wanted to check in with you since I have not heard anything back. Please advise whether It will be possible for you both to sign all of these and send them back soon. Thank you in advance for all of your time and effort.

Shannon

-----Original Message-----
From: Livingston, Shannon
Sent: Friday, March 12, 2004 3:50 PM
To: 'tblankenship1@austin.rr.com'
Cc: 'Schen4@austin.rr.com'
Subject: Corrected Formal Papers for 08211/0200253-US0/P05742 and 08211/0200254-US0/P05741

Hello - I have taken over responsibility for the above-referenced cases. I looked at the e-mails between Janice Kniep and yourself. I am forwarding to you the "new" Formal Papers for filing after the application has been filed. If you both could sign, fax back and return by mail as soon as is convenient for you I would greatly appreciate it. Thank you in advance for your time.

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Should you have any questions, please do not hesitate to email me.


Dec and POA.pdf
(57 KB)


Assignment.pdf (27 KB)


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(78 KB)

Assignment.pdf (24 KB)

Sincerely,

Shannon Livingston
Secretary
Darby & Darby P.C.
1191 Second Avenue
Seattle, WA 98101

206.262.8953 | direct
206.262.8901 | fax

http://www.darbylaw.com

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is described and claimed and for which a patent is sought on the invention entitled:

APPARATUS FOR CIRCUIT WITH KEEPER

the specification of which was filed on November 26, 2003 as Application No. 10/724,028.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to herein. I do not know and do not believe that the same was ever known or used in the United States of America before my or our invention thereof or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, or in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigned more than twelve months prior to this application.

I acknowledge the duty to disclose all information known to me that is material to patentability in accordance with Title 37, Code of Federal Regulations, § 1.56.

FOREIGN PRIORITY CLAIM

I hereby claim foreign priority benefits under Title 35, United States Code § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

[x] no such foreign applications have been filed

[ ] such foreign application have been filed as follows:

EARLIEST FOREIGN APPLICATION(S), IF ANY FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION

Application Number	Country	Date of Filing	Priority Claimed Under 35 USC 119
			___ Yes No ___

ALL FOREIGN APPLICATION(S), IF ANY FILED MORE THAN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION

Application Number	Country	Date of Filing

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[ ] such U.S. provisional application have been filed as follows:

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[x] no such U.S./PCT applications have been filed.

[ ] such U.S./PCT application have been filed as follows:

Application Number	Date of Filing	Status (Patented/Pending/Abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made

with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the practitioners under Customer Number

38845

all of **Darby & Darby P.C.**, P.O. Box 5257, New York, New York 10150-5257, jointly, and each of them severally, my attorneys at law/patent agent(s), with full power of substitution, delegation and revocation, to prosecute this application, to make alterations and amendments therein, to receive the patent, and to transact all business in the U. S. Patent and Trademark Office connected therewith.

Please mail all correspondence to John W. Branch, whose address is:

Darby & Darby P.C.
P.O. Box 5257
New York, New York 10150-5257

Please direct telephone calls to: John W. Branch at (206) 262-8900.

Please direct facsimiles to: (212) 753-6237

Full name of sole or first inventor Timothy L. Blankenship	
Sole or first inventor's signature	Date
Residence Austin, Texas	
Citizenship US	
Mailing Address 4613 Saloma Place Austin, Texas 78749	

Full name of second inventor, if any Sijian Chen	
Second inventor's signature	Date
Residence Austin, Texas	
Citizenship China	
Mailing Address 9114-B Sedgemoor Tr. Austin, Texas 78748	

Attorney Docket No.: 08211/0200253-US0

ASSIGNMENT

I, Timothy L. Blankenship, a citizen of US, residing at 4613 Saloma Place; Austin, Texas 78749; and

I, Sijian Chen, a citizen of China, residing at 9114-B Sedgemoor Tr.; Austin, Texas 78748;

and each of us, if more than one person is identified above (hereinafter "ASSIGNOR") in consideration of the sum of Ten Dollars ($10.00), or the equivalent thereof, and other good and valuable consideration, the sufficiency of which and receipt of which are hereby acknowledged, paid to ASSIGNOR by

National Semiconductor Corporation

a Corporation organized under the laws of Delaware, located at 2900 Semiconductor Drive, Santa Clara, California 95051-8090 (hereinafter "ASSIGNEE"), do hereby sell and assign to said ASSIGNEE, its successors and assigns, the below indicated right, title, and interest, **throughout the world** in and to my Invention entitled:

APPARATUS FOR CIRCUIT WITH KEEPER

invented by me and described in Patent Application No. 10/724,028, filed on November 26, 2003, in the United States; and all patents, divisions, reissues, continuations and any extensions thereof and rights of priority therein, said interest being my entire ownership interest in the same, to be held and enjoyed by said ASSIGNEE, its successors, assigns, or other legal representatives, to the full end of the term thereof, as fully and entirely as the same would have been held and enjoyed by me if this assignment and sale had not be made;

And for the consideration aforesaid, I hereby covenant and agree to and with said ASSIGNEE, its successors and assigns, that whenever ASSIGNEE, its counsel or representative, or the counsel or representative of its successors or assigns, shall advise that an amendment to, or

a division of, or any other proceeding or action in connection with an application concerning said Invention, including interference proceedings, is lawful and desirable, or that a reissue or continuation or extension of such application or patent issuing therefrom is lawful and desirable, I will sign all papers and drawings, take all rightful oaths and affidavits, and do all acts necessary or required to be done for the procurement of all lawful rights associated with the Invention, or for the reissue or continuation or extension of the same, will do all acts necessary or required to secure in said ASSIGNEE, its successors or assigns, the title to and full benefit of all rights hereby assigned, without charge to said ASSIGNEE or its successors or assigns, but at its or their expense; and I hereby appoint every present or future officer of said ASSIGNEE as my agent to sign all such papers and to do all such necessary acts on my behalf, to the fullest extent permitted by law;

And I hereby authorize and request the Commission of Patents and Trademarks and any other granting authority to issue any Letters Patent resulting from said Invention and application(s) concerning same to said ASSIGNEE.

This assignment shall have an effective date corresponding to the last date of execution.

I declare under penalty of perjury under the laws of the United States of America, and under penalty of the laws of any other jurisdiction before which this document may be presented, that I have signed this document as my own free act and that all of the foregoing is true and correct.

IN TESTIMONY WHEREOF, I have hereunto set my hand this _____ day of _____, 2004

_____
Timothy L. Blankenship

STATE OF _____)
)ss.
COUNTY OF _____)

On this _____ day of _____, 2004, before me personally appeared Timothy L. Blankenship to me known and known to me to be the person described in and who executed the foregoing instrument, and he duly acknowledged to me that he executed the same for the uses and purposes therein set forth.

[SEAL]

_____
Notary Public

IN TESTIMONY WHEREOF, I have hereunto set my hand this _____ day of _____, 2004

_____
Sijian Chen

STATE OF _____)
)ss.
COUNTY OF _____)

On this _____ day of _____, 2004, before me personally appeared Sijian Chen to me known and known to me to be the person described in and who executed the foregoing instrument, and he duly acknowledged to me that he executed the same for the uses and purposes therein set forth.

[SEAL]

_____
Notary Public

Livingston, Shannon

From: Gaffney Matthew
Sent: Friday, March 26, 2004 12:10 PM
To: 'Schen4@austin.rr.com'
Cc: Livingston, Shannon
Subject: Formal papers for 08211/0200253-US0

Hello Sijian,

We previously sent you formal papers for your signature for the "keeper transistor" patent. Please let me know whether you are willing to sign these documents. Also, please let me know if there is anything we can do to make it more convenient for you to sign them and get them back to us. For you convenience, I am re-sending the formal papers to you.


Dec and POA.pdf (53 KB)


Assignment.pdf (23 KB)

Attached please find: 1) a "corrected" Assignment and 2) a "corrected" Combined Declaration and Power of Attorney document. Please print the Assignment document (single-sided) and check that the information is correct. If the information is correct, please sign where indicated before a notary. Please print the Combined Declaration and Power of Attorney (single-sided) and also confirm the information is correct in this document. If the information is correct, please sign on the last page . Please return the signed documents by facsimile (fax number 206.262.8901) and by mail to Matthew Gaffney at Darby & Darby P.C., 1191 Second Avenue, Suite 1900, Seattle, Washington 98101. If there is incorrect information please let me know as soon as possible so we can correct the errors. We have a deadline of April 27, 2004 for filing these documents for "Missing Parts".

Should you have any questions, please do not hesitate to contact me.

Matthew M. Gaffney
Darby & Darby P.C.
1191 Second Avenue
Seattle, WA 98101

206.262.8910 | direct
206.262.8901 | fax
http://www.darbylaw.com

Kniep, Janice

From: Kniep, Janice
Sent: Thursday, November 20, 2003 2:32 PM
To: 'tblankenship1@austin.rr.com'
Cc: 'schen4@austin.rr.com'; Gaffney Matthew
Subject: NSC applications and papers for signature P05741 and P05742

Dear Mr. Blankenship,

I have attached the application, drawings and formal papers for P05741 for your signature. Please review and sign the Declaration and Assignment documents where indicated. Please return the signed documents via email or fax (we thought it might be more convenient for you to scan and email the signed documents back rather than faxing) and send the originals back to my attention at the address given below.

I have also attached the application, drawings and formal papers for P05742 for your and Mr. Chen's signatures. It is my understanding that you will print the documents, sign and obtain Mr. Chen's signature as well. Please return the signed documents as indicated above.

If you or Mr. Chen have any questions, please contact me or Matt Gaffney.

I would like to thank you and Mr. Chen in advance for your kind assistance. It is very much appreciated.

Best Regards,

Janice Kniep
Legal Secretary
Darby & Darby P.C.
1191 Second Avenue
Seattle, WA 98101

206-262-8953 | direct
206-262-8901 | fax

http://www.darbylaw.com

Livingston, Shannon

From: Sijian Chen [schen4@austin.rr.com]
Sent: Sunday, March 28, 2004 2:31 PM
To: Gaffney Matthew
Cc: Livingston, Shannon
Subject: Re: Formal papers for 08211/0200253-US0

Matthew, Shannon,

I was let go by National at a difficult time of my life when I just had a new child and my wife was still sick at home. As much as I'd like to help National out completing the patent applications, I have many other obligations that's at higher priority. I'm afraid I do not have any time at the present to review the papers. Please remove my e-mail address and contact information from your contact list.

Rgs,

Sijian

----- Original Message -----
From: Gaffney Matthew
To: Schen4@austin.rr.com
Cc: Livingston, Shannon
Sent: Friday, March 26, 2004 2:09 PM
Subject: Formal papers for 08211/0200253-US0

Hello Sijian,

We previously sent you formal papers for your signature for the "keeper transistor" patent. Please let me know whether you are willing to sign these documents. Also, please let me know if there is anything we can do to make it more convenient for you to sign them and get them back to us. For you convenience, I am re-sending the formal papers to you.

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Matthew M. Gaffney

Darby & Darby P.C.

1191 Second Avenue

Seattle, WA 98101

206.262.8910 | direct

206.262.8901 | fax

http://www.darbylaw.com

Livingston, Shannon

From: Gaffney Matthew
Sent: Monday, March 29, 2004 11:18 AM
To: 'Sijian Chen'
Cc: Livingston, Shannon
Subject: RE: Formal papers for 08211/0200253-US0

Sijian,

I understand that you may be reluctant to help National under the circumstances, and have other obligations that have higher priority.

We need to have either your signature on the declaration and the assignment, or proof that you refuse to execute these documents. If you are willing to sign these documents, please do so. If you refuse to do so, I would greatly appreciate it if you would mail us a letter stating that you refuse to execute the declaration and the assignment for Patent Application 10/724,028, filed on November 26, 2003, entitled "APPARATUS FOR CIRCUIT WITH KEEPER". Please mail the signed documents, or a letter stating your refusal, to Matthew Gaffney at Darby & Darby P.C., 1191 Second Avenue, Suite 1900, Seattle, Washington 98101.

Regards,
Matt

-----Original Message-----
From: Sijian Chen [mailto:schen4@austin.rr.com]
Sent: Sunday, March 28, 2004 2:31 PM
To: Gaffney Matthew
Cc: Livingston, Shannon
Subject: Re: Formal papers for 08211/0200253-US0

Matthew, Shannon,

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Rgs,

Sijian

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From: Gaffney Matthew
To: Schen4@austin.rr.com
Cc: Livingston, Shannon
Sent: Friday, March 26, 2004 2:09 PM
Subject: Formal papers for 08211/0200253-US0

Hello Sijian,

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Should you have any questions, please do not hesitate to contact me.

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NEW YORK, NY 10022-7513
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April 20, 2004

Reference: 08211/0200253-US0

MATTHEW M. GAFFNEY
ATTORNEY AT LAW
206.262.8910
mgaffney@darbylaw.com

VIA FEDERAL EXPRESS

Sijian Chen
9114-B Sedgemoor Tr.
Austin, TX 78748

Re: **URGENT - Formal Papers for execution and return**

Dear Mr. Chen:

Enclosed please find a copy of the Application and Drawings as filed for the above-identified matter, for which you are a named inventor. Also enclosed is a copy of a notice received from the U.S. Patent and Trademark Office (USPTO) indicating that certain items are missing from the application as filed. The due date for filing these items is April 26, 2004.

We are also enclosing a Combined Declaration and Power of Attorney and an Assignment of this application for execution by you. If minor changes need to be made to correct for, *e.g.*, typographical errors, they can be made in pen. However, all such changes must be ***initialed and dated.***

Please return the executed documents to us (in the pre-paid Federal Express envelope) for filing with the USPTO no later than April 23, 2004. If you have any questions or comments, please do not hesitate to contact me.

Very truly yours,

Matthew M. Gaffney

MMG/ln

Enclosures

08211/0200253-US0/P05742

APPARATUS FOR CIRCUIT WITH KEEPER

Field of the Invention

The invention related to a keeper circuit. In particular, the invention related to a keeper circuit for ensuring that the high-range and low-range outputs of a circuit utilizing voltage doubling techniques are actively driven.

Background

Voltage doubling is a technique that makes it possible to design electrical circuits that operate with high power supply voltages (e.g. 10V or above), while not allowing the Vgs, Vgd, or Vds of the individual transistors in the circuit to exceed a lower value, such as 5V. The voltage doubling technique is often implemented with cascode transistors. In general, voltage doubling techniques may be used to extend the operating range to approximately 2X volts, where the underlying components can withstand X volts.

Brief Description of the Drawings

Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following drawings, in which:

Figure 1 illustrates a schematic diagram of a circuit that includes a keeper switch;

Figure 2 shows a schematic diagram of an exemplary embodiment of the circuit of Figure 1;

Figure 3 illustrates a schematic diagram of an exemplary embodiment of an inverter circuit with a keeper switch;

Figure 4 shows a schematic diagram of another exemplary embodiment of an inverter circuit with a keeper switch;

Figure 5 illustrates a schematic diagram of an exemplary embodiment of a level translator circuit with a keeper switch;

Figure 6 shows a schematic diagram of another exemplary embodiment of a level translator circuit with a keeper switch; and

Figure 7 illustrates a schematic diagram of another exemplary embodiment of a level translator circuit with a keeper switch, arranged in accordance with aspects of the present invention.

Detailed Description

Various embodiments of the present invention will be described in detail with reference to the drawings, where like reference numerals represent like parts and assemblies throughout the several views. Reference to various embodiments does not limit the scope of the invention, which is limited only by the scope of the claims attached hereto. Additionally, any examples set forth in this specification are not intended to be limiting and merely set forth some of the many possible embodiments for the claimed invention.

Throughout the specification and claims, the following terms take at least the meanings explicitly associated herein, unless the context clearly dictates otherwise. The meanings identified below are not intended to limit the terms, but merely provide illustrative examples for the terms. The meaning of "a," "an," and "the" includes plural reference, the meaning of "in" includes "in" and "on." The term "connected" means a direct electrical connection between the items connected, without any intermediate devices. The term "coupled" means either a direct electrical connection between the items connected, or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means either a single component or a multiplicity of components, either active and/or passive, that are coupled together to provide a desired function. The term "signal" means at least one current, voltage, charge, temperature, data, or other signal.

Briefly stated, the invention is related to a circuit with a keeper switch that is configured to minimize capacitive coupling between the gate and drain of a transistor arranged in a cascode configuration. The keeper switch is coupled between the source and gate of the cascode transistor. The keeper switch is active if a voltage at the drain of the keeper switch circuit corresponds to a first logic level. If this event occurs, the source and gate of the cascode transistor are coupled together.

Figure 1 illustrates a block diagram of a circuit (100) that includes a keeper switch circuit. Circuit 100 includes a first transistor (M0) and a second transistor (M1) configured in a cascode arrangement (104), and a keeper switch circuit (102). The second transistor (M1) has a gate that is coupled to a bias node (N12), a drain that is coupled to a first output node (N1), and a source that is coupled to a second output node (N2). The keeper switch circuit (102) has three terminals that are respectively coupled to the gate of the second transistor (M1), the drain of second transistor (M1), and the source of the second transistor (M1). The second transistor (M1) is configured to receive a first cascode bias voltage (bias) at the bias node (N12). The first cascode bias voltage (signal bias) is suitable as a cascode bias voltage.

The keeper switch circuit (102) is configured to influence a resistance between the second output node (N2) and the bias node (N12) in response to a control signal (e.g. signal bias). The keeper switch circuit (102) is configured to couple the second output node (N2) to the bias node (N12) if the control signal corresponds to a first logic level. The keeper switch circuit (102) is further configured to isolate the second output node (N2) from the bias node (N12) if the control signal corresponds to a second logic level.

In Figure 2, circuit 200 is a particular implementation of circuit 100, where the keeper switch circuit (102) is implemented by a transistor (M8). Transistor M8 has a gate that is coupled to the first output node (N1), a source that is coupled to the second output node (N2), and a drain that is coupled to the bias node (N12). Alternatively, the drain may be coupled to the second output node (N2), and the source may be coupled to the bias node (N12).

Figure 3 illustrates a schematic diagram of a circuit (300) that is an exemplary implementation of circuit 100. Circuit 300 is a high-voltage inverter that utilizes voltage doubling techniques. Circuit 300 includes transistors M2-M3 and M6-M7, and keeper switch circuit 102. Keeper switch circuit 102 is implemented by transistor M8. Transistor M8 has a gate that is coupled to node N1, a source that is coupled to node N2, and a drain that is coupled to node N11.

Transistors M2 and M3 are each arranged to operate as a cascode transistor. Transistor M2 is configured to receive a first bias signal Vsp at a gate of transistor M2 (node N11), and transistor M3 is configured to receive a second bias signal Vsn at a gate

of transistor M3 (node N13). Signal Vsp is a cascode bias voltage that is used to bias transistor M2, and signal Vsn is a cascode bias voltage that is used to bias transistor M3. The voltages associated with signals Vsp and Vsn are set by several factors including the power supply voltage, the maximum Vgs, Vgd, and Vds of the process for relatively long-term reliability, the threshold voltages of the transistors, the junction diode breakdowns of the transistors, and the input voltage swing. Signals Vsp and Vsn are selected such that the maximum Vgs, Vgd, and Vds of the transistors for relatively long-term reliability are not exceeded.

Transistor M6 is configured to receive a high-range signal in_hr at the gate of transistor M6, and transistor M7 is configured to receive a low-range signal in_lr at the gate of transistor M7. Signal in_lr is bounded between 0 volts and approximately Vdda/2, where Vdda is the voltage associated with the power supply. Signal in_hr is bounded between Vdda and approximately Vdda/2. Signal in_hr and signal in_lr each correspond to substantially the same logic level at approximately the same time. A high-range output signal (hr) is provided at the drain of transistor M6 (node N2). The logic level associated with signal hr corresponds to the inverse of the logic level of signals in_lr and in_hr. Circuit 300 is also configured to provide a full-range output signal (fr) at the source of transistor M2 (node N1), and a low-range output signal (lr) at the source of transistor M3 (node N3). Signals fr and lr each correspond to the same logic level as signal hr, but are bounded over different ranges. Signal lr is bounded between 0 volts and approximately Vdda/2, signal hr is bounded between approximately Vdda/2 and Vdda, and signal fr is bounded between 0 volts and Vdda.

Transistor M8 is configured to ensure that signal hr is actively driven regardless of the voltage associated with signals in_hr and in_lr, even at initial power-on. Transistor M8 is arranged for preventing charge injection (i.e. capacitive coupling) that could otherwise be caused as a result of the gate-to-drain capacitance on transistor M6. If present, injected charge could cause a voltage at the gate of transistor M6 to move outside of the desired operating range for Vgs, Vds, and Vgd of transistors M6. According to the example illustrated in Figure 3, transistor M2 is a p-type transistor, and transistor M8 is a p-type transistor.

Figure 4 illustrates a schematic diagram of a circuit (400) that is another exemplary implementation of Figure 1. Circuit 400 is substantially similar to circuit 300 in some ways, albeit different in other ways. In circuit 400, keeper switch circuit 102 is implemented by transistor M9. Transistor M9 has a gate that is coupled to node N1, a drain that is coupled to node N13, and a source that is coupled to node N3.

Transistor M9 is configured to ensure that signal lr is actively driven independent of the voltage associated with signals in_hr and in_lr, including at the initial power-on state. Transistors M3 and M9 are n-type transistors.

Figure 5 illustrates a schematic diagram of a level-shifter circuit (500). Circuit 500 includes transistors M2-M5 and M11-M16, keeper circuit 102 (transistor M8) and another keeper circuit (transistor M10). Transistor M4 has a gate that is coupled to node N11, a drain that is coupled to a first complement output node N21, and a source that is coupled to a second complement output node N22. Transistor M10 has a gate that is coupled to node N21, a source that is coupled to node N22, and a drain that is coupled to node N11.

Transistor M8 is configured to operate in a substantially similar manner as described with regard to Figure 3, albeit different in some ways. Transistor M4 is arranged to operate as a cascode transistor in cooperation with transistor M12. Transistor M5 is configured to operate as a cascode transistor in cooperation with transistor M14. Circuit 500 is configured to provide signals hr, fr, lr, hrb, frb, and lrb in response to a data input signal (din). Signal hrb is a complement of signal hr, signal frb is a complement of signal fr, and signal lrb is a complement of signal lr. As an example, transistors M2, M4, M8, and M10 are each p-type transistors. Transistor M8 is configured to ensure that signal hr is actively driven regardless of the voltage associated with signal din. Transistor M10 is configured to ensure that signal hrb is actively driven regardless of the voltage associated with signal din.

Figure 6 illustrates a schematic diagram of a circuit (600) that is substantially similar to circuit 500, albeit different in some ways. In this embodiment, the keeper circuit 102 is implemented by transistor M9, and the other keeper circuit is implemented by transistor M17. In this example, transistors M3, M5, M9, and M17 are n-type

transistors. Transistor M9 is configured to ensure that signal lr is actively driven. Transistor M17 is configured to ensure that signal lrb is actively driven.

Figure 7 illustrates a schematic diagram of a circuit (700) that is substantially similar to circuit 600, albeit different in some ways. In this embodiment, keeper circuit 102 is implemented by transistor M19, and the other keeper circuit is implemented by transistor M18. Keeper switch circuit 102 and the other keeper switch circuit are each coupled respectively to nodes N3, N13, and M23. Transistor M19 has a gate that is coupled to node N23, a source that is coupled to node N13, and a drain that is coupled to node N3. Transistor M18 has a gate that is coupled to node N3, a source that is coupled to node N13, and a drain that is coupled to node N23.

In this example, keeper switch circuit 102 is configured to influence a resistance between nodes N3 and M13. Keeper switch circuit 102 is configured to receive a control signal (e.g. signal lrb at node N23). Also, the keeper switch circuit 102 is further configured to couple node N3 to node N13 if the control signal corresponds to a first logic level (e.g. low). Additionally, keeper switch circuit 102 is further configured to isolate node N3 from node N13 if the control signal corresponds to a second logic level (e.g. high). In this example, transistors M3 and M5 are n-type transistors, and transistor M18 and M19 are p-type transistors.

The above specification, examples and data provide a description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention also resides in the claims hereinafter appended.

What is claimed is:

1. A circuit comprising:

a first transistor;

a second transistor that is arranged to operate as a cascode transistor in cooperation with the first transistor; and

a keeper switch circuit including three terminals that are respectively coupled to a gate, a drain, and a source of the second transistor.

2. The circuit of Claim 1, wherein

the second transistor is configured to receive a first cascode bias voltage at the gate of the second transistor, and wherein

the first cascode bias voltage is suitable for biasing a cascode transistor.

3. The circuit of Claim 1, wherein

the keeper switch circuit is configured to influence a resistance between the source and the gate of the second transistor in response to a control signal.

4. The circuit of Claim 1, wherein

the keeper switch circuit is configured to:

receive a control signal at the drain of the second transistor; and

couple the source of the second transistor to the gate of the second transistor if the control signal corresponds to a first logic level.

5. The circuit of Claim 4, wherein

the keeper switch circuit is further configured to isolate the source of the second transistor from the gate of the second transistor if the control signal corresponds to a second logic level.

6. The circuit of Claim 1, wherein

the keeper switch circuit comprises a keeper transistor including:

a gate that is coupled to the drain of the second transistor;

a source that is coupled to one of the source of the second transistor and the gate of the second transistor; and

a drain that is coupled to the other of the source of the second transistor and the gate of the second transistor.

7. The circuit of Claim 6, wherein

the second transistor is one of an n-type transistor and a p-type transistor, and the keeper transistor is the one of the n-type transistor and the p-type transistor.

8. The circuit of Claim 6, wherein

the second transistor is one of an n-type transistor and the p-type transistor, and the keeper transistor is the other of the n-type transistor and the p-type transistor.

9. The circuit of Claim 1, further comprising:

a third transistor;

a fourth transistor that is arranged to operate as a cascode transistor in cooperation with the third transistor; and

another keeper switch circuit including three terminals that are respectively coupled to a gate, a drain, and a source of the fourth transistor.

10. The circuit of Claim 9, wherein

the other keeper switch circuit comprises a fifth transistor including:

a gate that is coupled to the drain of the fourth transistor,

a source that is coupled to one of the source of the fourth transistor and the gate of the second transistor, and

a drain that is coupled to the other of the source of the fourth transistor and the gate of the second transistor.

11. A logic circuit comprising:

a first transistor;

a second transistor that is arranged to operate as a cascode transistor in cooperation with the first transistor, wherein the second transistor includes:

a gate that is coupled to a bias node,

a drain that is coupled to a first output node, and

a source that is coupled to a second output node;

a third transistor;

a fourth transistor that is arranged to operate as a cascode transistor in cooperation with the third transistor, wherein the fourth transistor includes:

a gate that is coupled to the bias node,

a drain that is coupled to a first complement output node, and

a source that is coupled to a second complement output node,

a first keeper switch circuit that is coupled to the bias node, the second complement output node, and the second output node, and

a second keeper switch circuit that is coupled to the bias node, second output node, and the second complement output node.

12. The logic circuit of Claim 11, wherein

the second transistor is configured to receive a first cascode bias voltage at the bias node, wherein

the first cascode bias voltage is suitable for biasing a cascode transistor.

13. The logic circuit of Claim 11, wherein

the first keeper switch circuit is configured to influence a resistance between the second output node and the bias node in response to a control signal.

14. The logic circuit of Claim 11, wherein

the first keeper switch circuit is configured to:

receive a control signal at the second complement output node;

couple the second output node to the bias node if the control signal corresponds to a first logic level; and

isolate the second output node from the bias node if the control signal corresponds to a second logic level.

15. The logic circuit of Claim 11, wherein

the logic circuit is arranged to operate as a level shifter circuit.

16. The logic circuit of Claim 11, wherein

the first keeper switch circuit comprises a keeper transistor including:

a gate that is coupled to the second complement output node,

a source that is coupled to one of the second output node and the bias node, and

a drain that is coupled to the other of the second output node and the bias node.

17. The logic circuit of Claim 16, wherein

the second transistor is one of an n-type transistor and a p-type transistor, and the keeper transistor is the other of the n-type transistor and the p-type transistor.

18. The logic circuit of Claim 11, wherein

the second keeper switch circuit comprises a fifth transistor including:

a gate that is coupled to the second output node,

a source that is coupled to one of the second complement output node and the bias node, and

a drain that is coupled to the other of the second complement output node and the bias node.

19. The logic circuit as in Claim 18, wherein

the first keeper switch circuit comprises a keeper transistor, and

wherein the second transistor is one of an n-type transistor and a p-type transistor, the keeper transistor is the other of the n-type transistor and the p-type transistor, and the fifth transistor is the other of the n-type transistor and the p-type transistor.

20. A circuit comprising:

a transistor that is configured as a cascode transistor; and

means for coupling a source of the transistor to a gate of the transistor if a voltage associated with a drain of the transistor corresponds to a first logic level.

Abstract

A keeper switch circuit is configured to minimize capacitive coupling between the gate and drain of a cascode transistor. The keeper switch circuit is coupled between the source and gate of a cascode transistor. The keeper switch circuit is on if a voltage at the drain of the keeper switch circuit corresponds to a first logic level. The source and gate of the cascode transistor are coupled together if the keeper switch circuit is on.

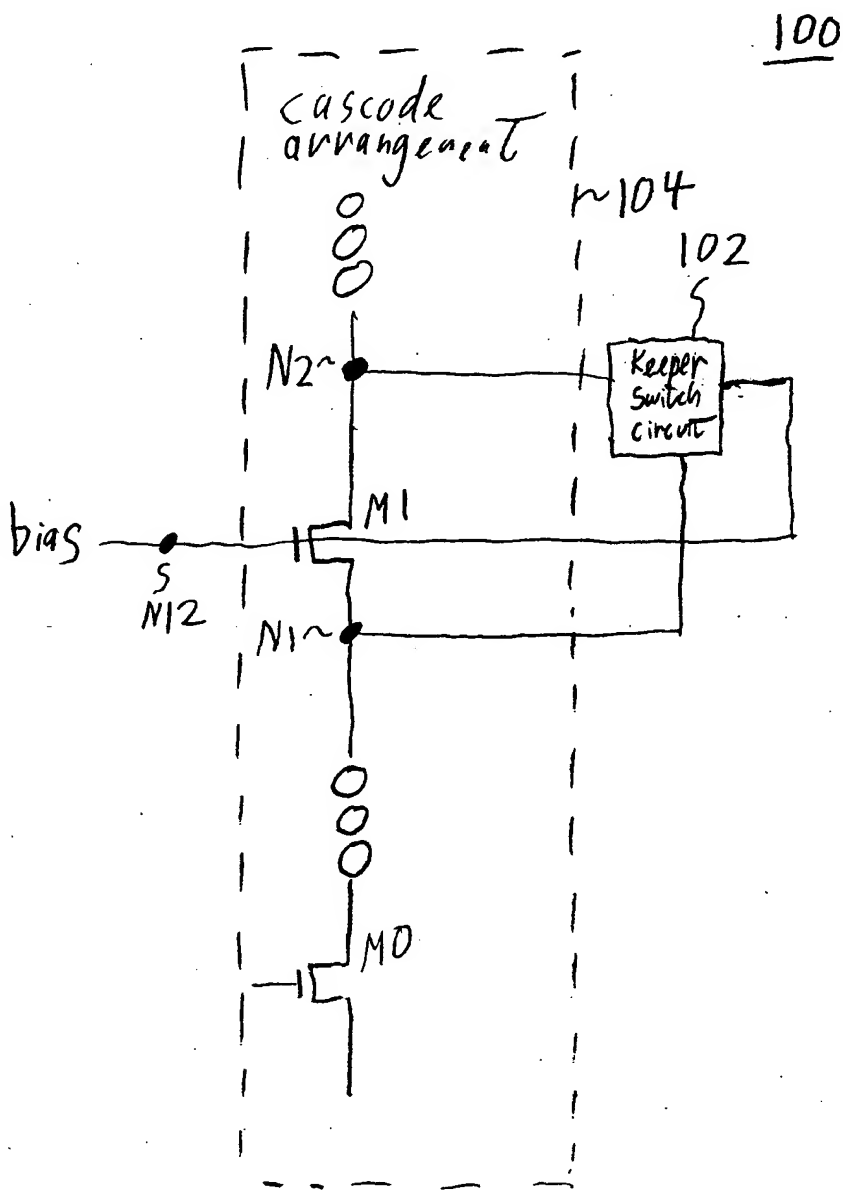
100
cascode arrangement
104
102
N2
Keeper Switch circuit
M1
bias
N12
N1
M0

Figure 1

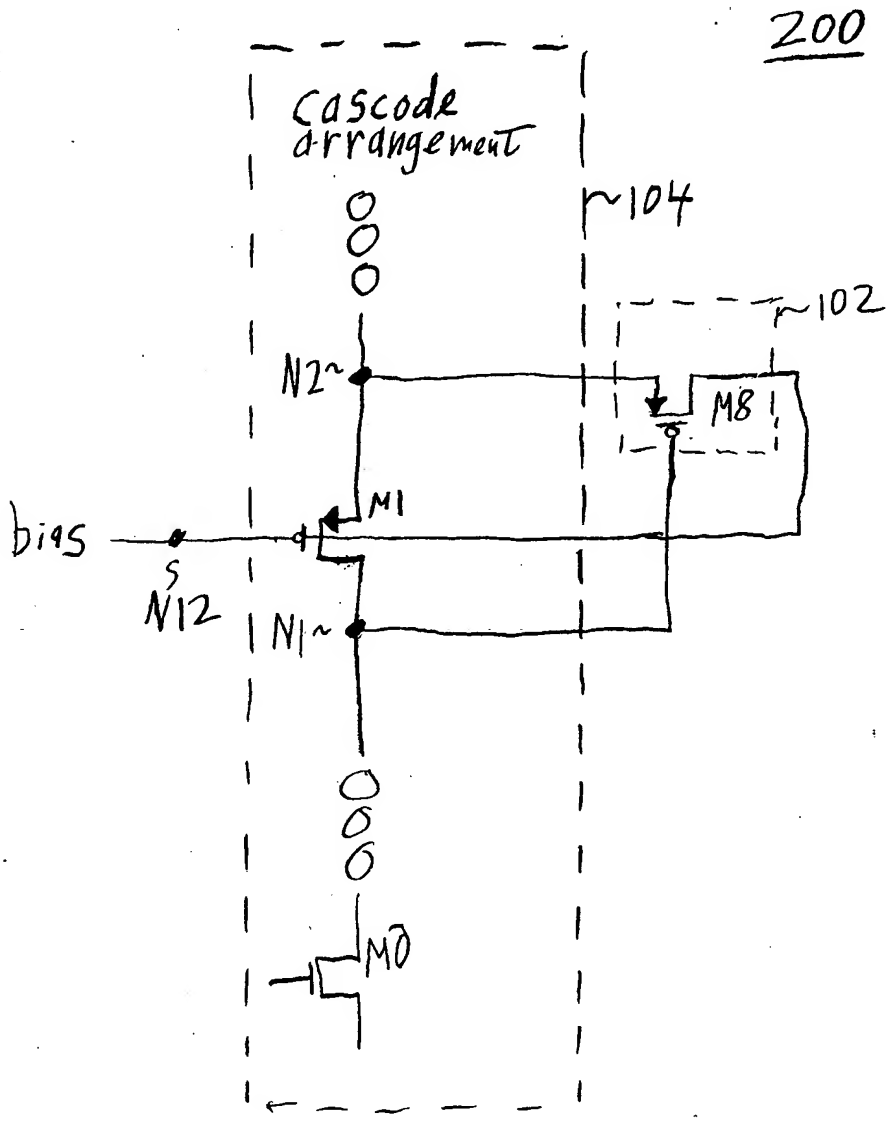

Figure 2

300

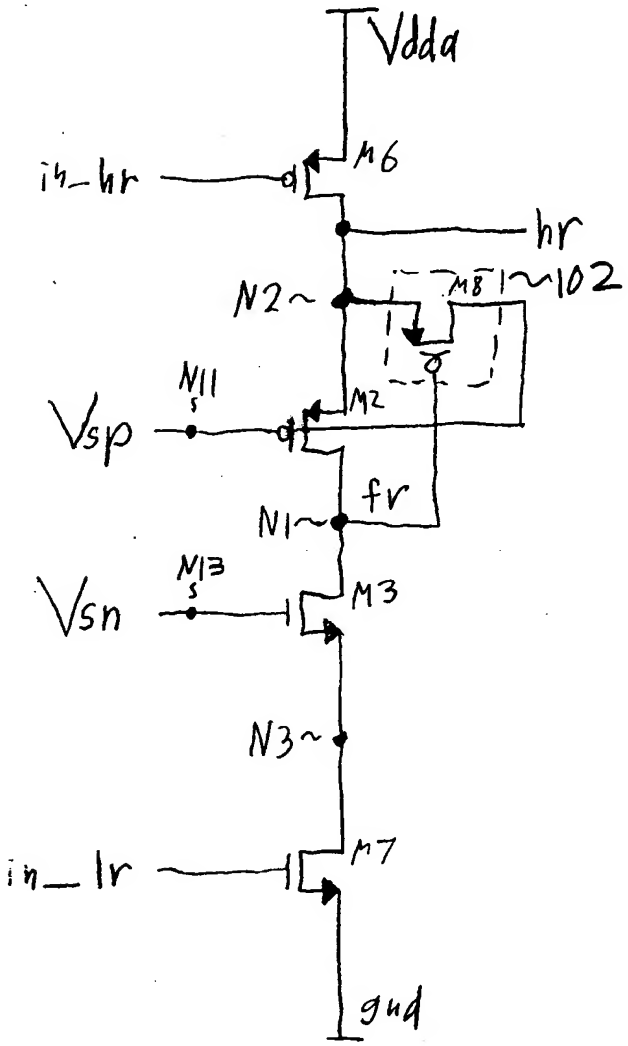
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Figure 3

400

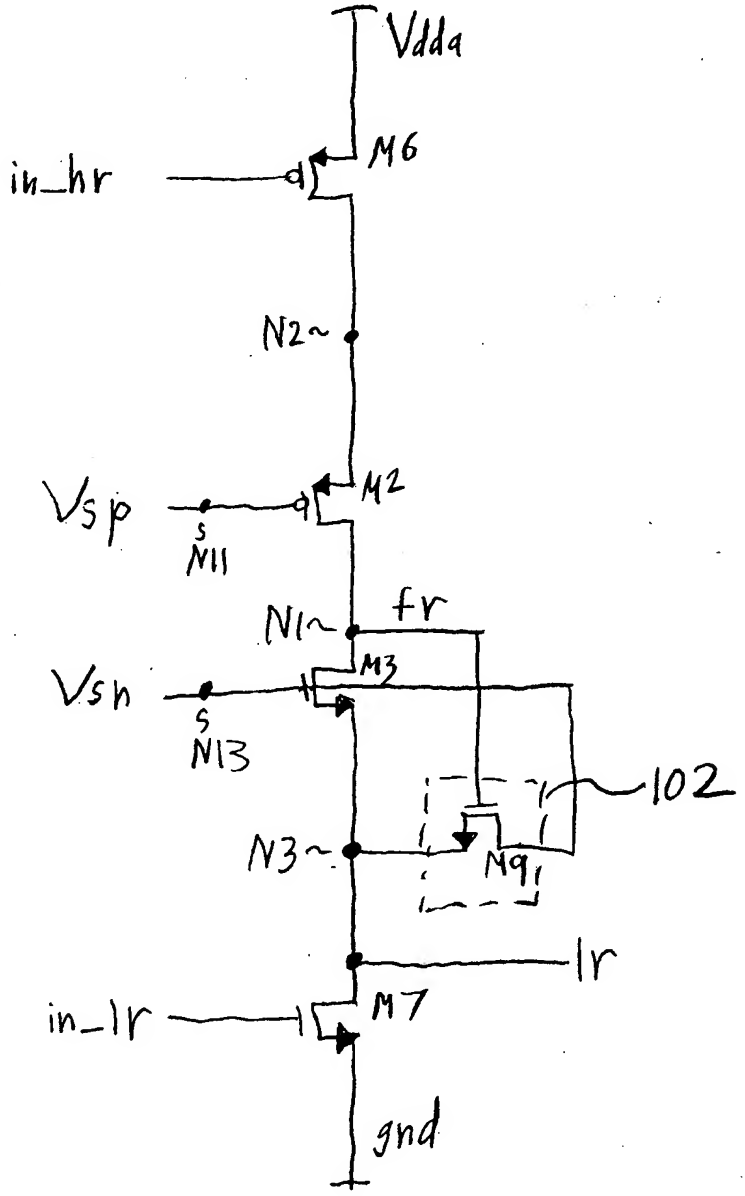

Figure 4

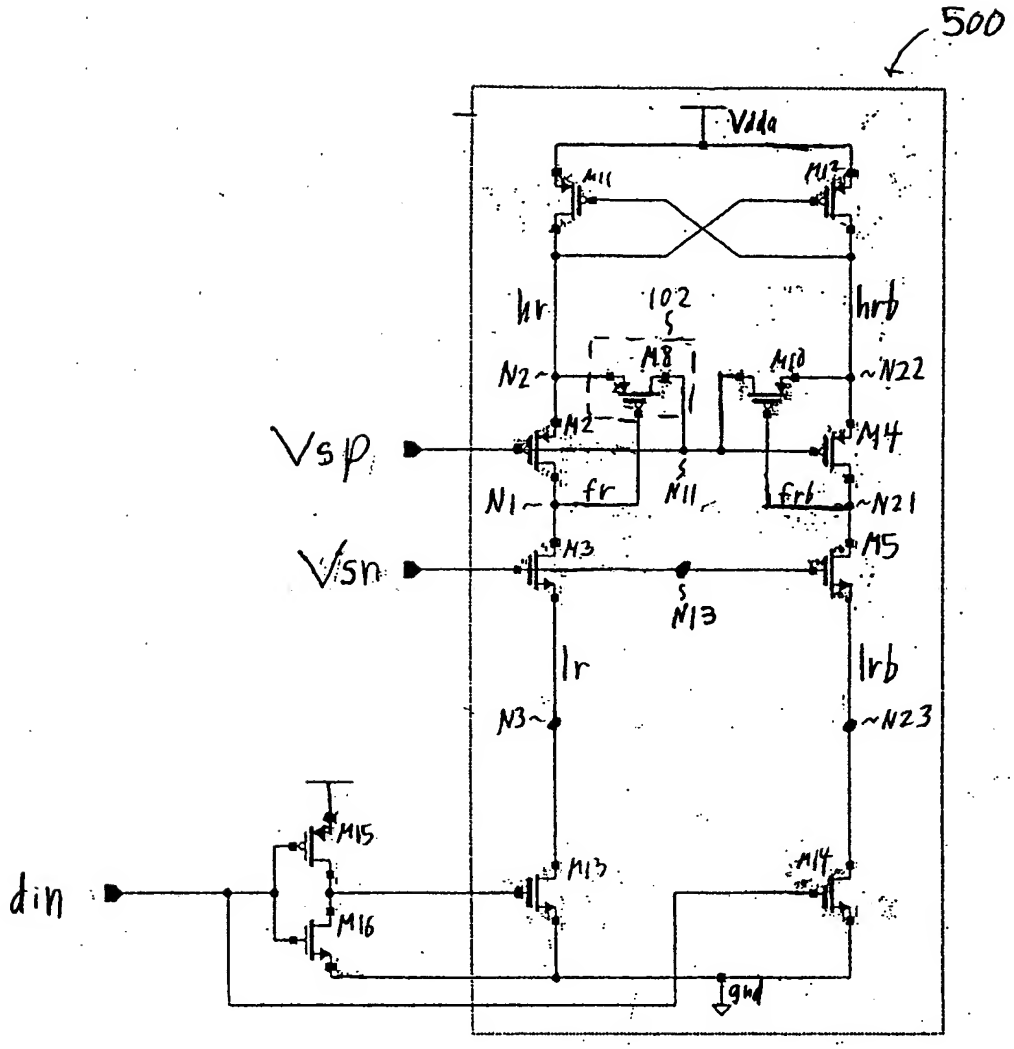
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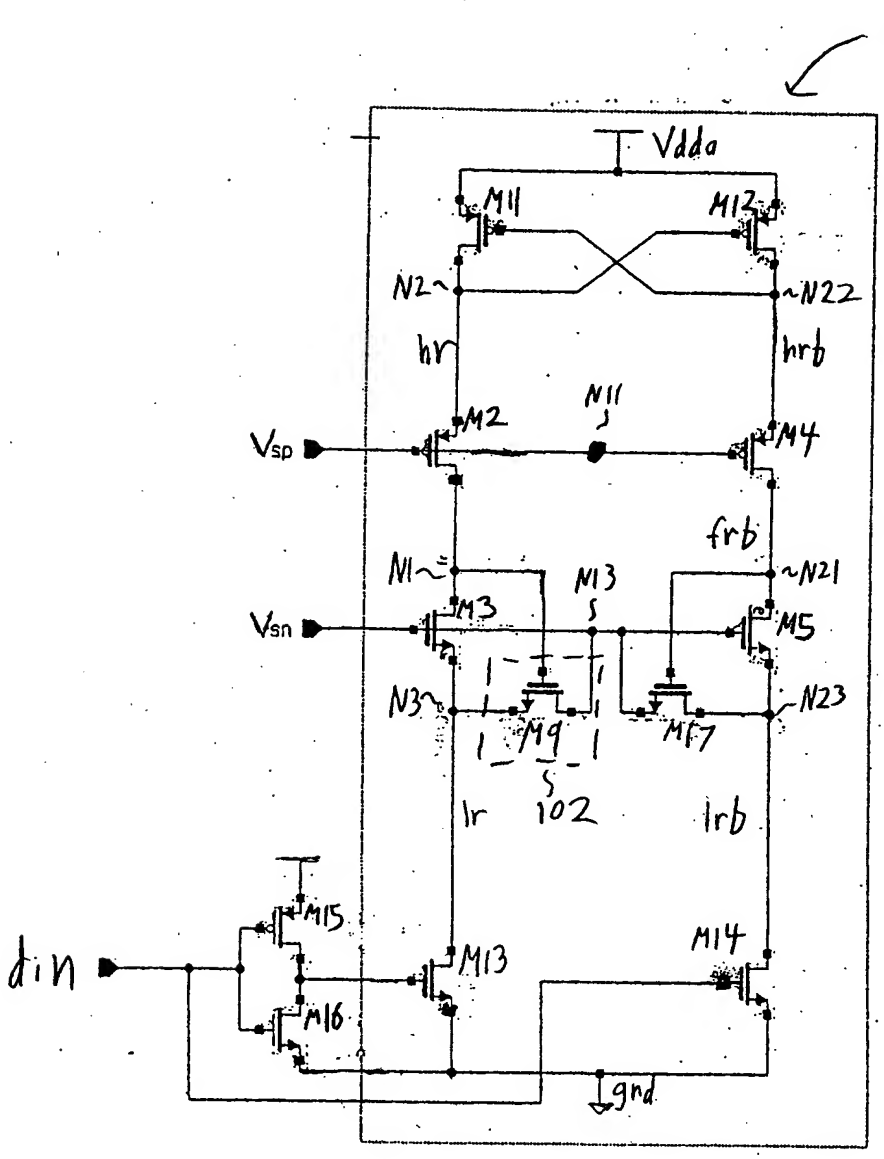
Figure 5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N21
M3
Vsn
M5
N3
N23
M9
M7
lr
102
lrb
M15
M14
din
M13
M16
gnd

Figure 6

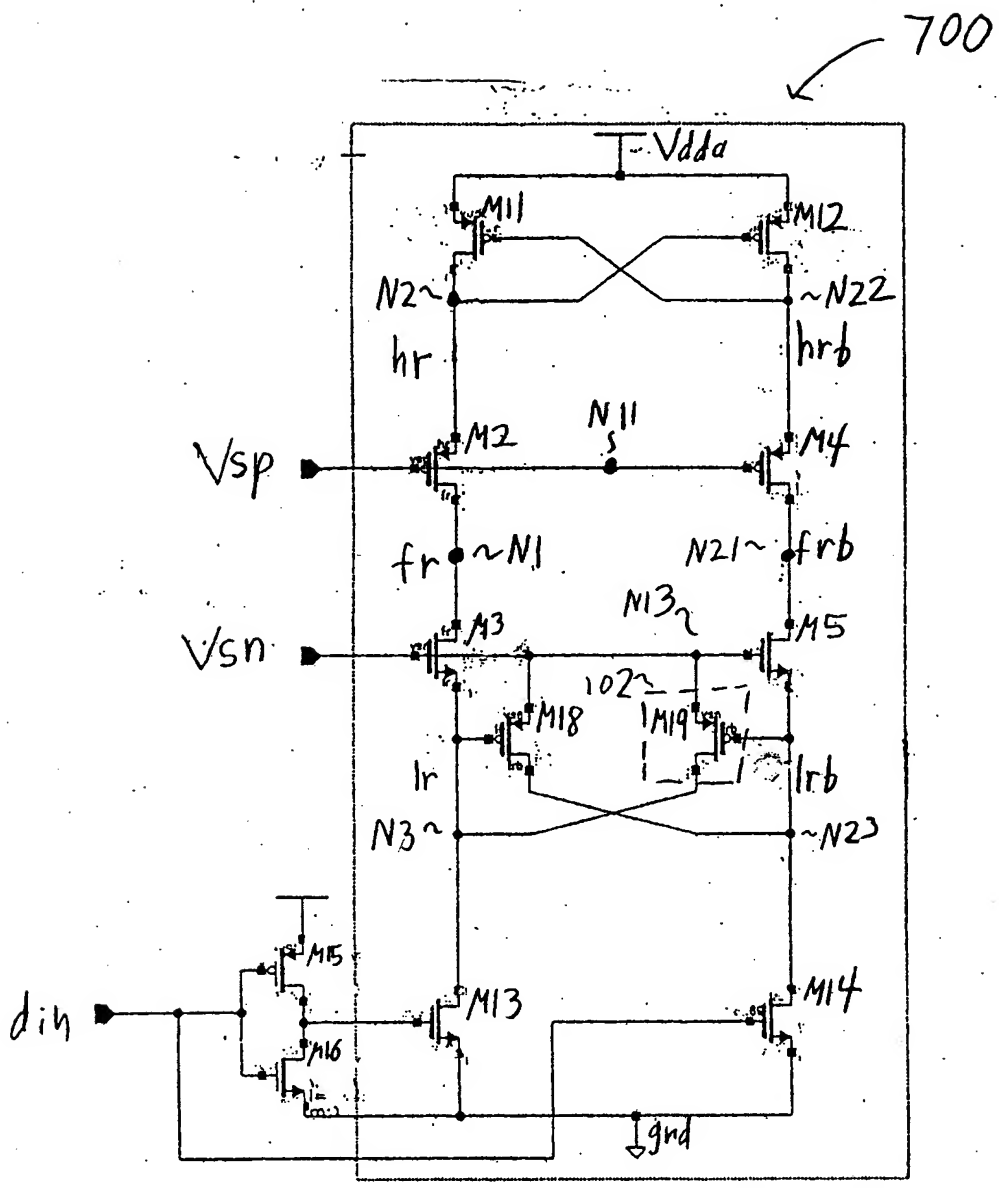

700
Vdda
M11
M12
N2
~N22
hr
hrb
Vsp
M2
N11
M4
fr
~N1
N21~
frb
N13
Vsn
M3
M5
102
M18
M19
lr
lrb
N3
~N23
M15
din
M13
M14
M16
gnd

Figure 7

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is described and claimed and for which a patent is sought on the invention entitled:

APPARATUS FOR CIRCUIT WITH KEEPER

the specification of which was filed on November 26, 2003 as Application No. 10/724,028.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to herein. I do not know and do not believe that the same was ever known or used in the United States of America before my or our invention thereof or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, or in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigned more than twelve months prior to this application.

I acknowledge the duty to disclose all information known to me that is material to patentability in accordance with Title 37, Code of Federal Regulations, § 1.56.

FOREIGN PRIORITY CLAIM

I hereby claim foreign priority benefits under Title 35, United States Code § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

[x] no such foreign applications have been filed

[ ] such foreign application have been filed as follows:

EARLIEST FOREIGN APPLICATION(S), IF ANY FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION

Application Number	Country	Date of Filing	Priority Claimed Under 35 USC 119
			___ Yes No ___

ALL FOREIGN APPLICATION(S), IF ANY FILED MORE THAN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION

Application Number	Country	Date of Filing

CLAIM FOR BENEFIT OF EARLIER U.S. PROVISIONAL APPLICATIONS

I hereby claim priority benefits under Title 35, United States Code §119(e), of any United States provisional patent application(s) listed below:

[x] no such U.S. provisional applications have been filed.

[ ] such U.S. provisional application have been filed as follows:

Application Number	Date of Filing	Priority Claimed Under 35 USC 119
		___ Yes No ___

CLAIM FOR BENEFIT OF EARLIER U.S./PCT APPLICATION(S)

I hereby claim the benefit under Title 35, United States Code, §120 of the United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose all information that is material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56 which became available to me between the filing date of the prior application and the national or PCT international filing date of this application:

[x] no such U.S./PCT applications have been filed.

[ ] such U.S./PCT application have been filed as follows:

Application Number	Date of Filing	Status (Patented/Pending/Abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made

with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the practitioners under Customer Number

38845

all of **Darby & Darby P.C.**, P.O. Box 5257, New York, New York 10150-5257, jointly, and each of them severally, my attorneys at law/patent agent(s), with full power of substitution, delegation and revocation, to prosecute this application, to make alterations and amendments therein, to receive the patent, and to transact all business in the U. S. Patent and Trademark Office connected therewith.

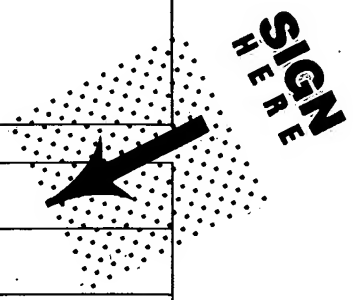
Please mail all correspondence to John W. Branch, whose address is:

Darby & Darby P.C.
P.O. Box 5257
New York, New York 10150-5257

Please direct telephone calls to: John W. Branch at (206) 262-8900.

Please direct facsimiles to: (212) 753-6237

Full name of sole or first inventor Timothy L. Blankenship	
Sole or first inventor's signature	Date
Residence Austin, Texas	
Citizenship US	
Mailing Address 4613 Saloma Place Austin, Texas 78749	



Full name of second inventor, if any Sijian Chen	
Second inventor's signature	Date
Residence Austin, Texas	
Citizenship China	
Mailing Address 9114-B Sedgemoor Tr. Austin, Texas 78748	

Attorney Docket No.: 08211/0200253-US0

ASSIGNMENT

I, Timothy L. Blankenship, a citizen of US, residing at 4613 Saloma Place; Austin, Texas 78749; and

I, Sijian Chen, a citizen of China, residing at 9114-B Sedgemoor Tr.; Austin, Texas 78748;

and each of us, if more than one person is identified above (hereinafter "ASSIGNOR") in consideration of the sum of Ten Dollars ($10.00), or the equivalent thereof, and other good and valuable consideration, the sufficiency of which and receipt of which are hereby acknowledged, paid to ASSIGNOR by

National Semiconductor

a Corporation organized under the laws of Delaware, located at 2900 Semiconductor Drive, Santa Clara, California 95051-8090 (hereinafter "ASSIGNEE"), do hereby sell and assign to said ASSIGNEE, its successors and assigns, the below indicated right, title, and interest, **throughout the world** in and to my Invention entitled:

APPARATUS FOR CIRCUIT WITH KEEPER

invented by me and described in Patent Application No. 10/724,028, filed on November 26, 2003, in the United States; and all patents, divisions, reissues, continuations and any extensions thereof and rights of priority therein, said interest being my entire ownership interest in the same, to be held and enjoyed by said ASSIGNEE, its successors, assigns, or other legal representatives, to the full end of the term thereof, as fully and entirely as the same would have been held and enjoyed by me if this assignment and sale had not be made;

And for the consideration aforesaid, I hereby covenant and agree to and with said ASSIGNEE, its successors and assigns, that whenever ASSIGNEE, its counsel or representative, or the counsel or representative of its successors or assigns, shall advise that an amendment to, or

a division of, or any other proceeding or action in connection with an application concerning said Invention, including interference proceedings, is lawful and desirable, or that a reissue or continuation or extension of such application or patent issuing therefrom is lawful and desirable, I will sign all papers and drawings, take all rightful oaths and affidavits, and do all acts necessary or required to be done for the procurement of all lawful rights associated with the Invention, or for the reissue or continuation or extension of the same, will do all acts necessary or required to secure in said ASSIGNEE, its successors or assigns, the title to and full benefit of all rights hereby assigned, without charge to said ASSIGNEE or its successors or assigns, but at its or their expense; and I hereby appoint every present or future officer of said ASSIGNEE as my agent to sign all such papers and to do all such necessary acts on my behalf, to the fullest extent permitted by law;

And I hereby authorize and request the Commission of Patents and Trademarks and any other granting authority to issue any Letters Patent resulting from said Invention and application(s) concerning same to said ASSIGNEE.

This assignment shall have an effective date corresponding to the last date of execution.

I declare under penalty of perjury under the laws of the United States of America, and under penalty of the laws of any other jurisdiction before which this document may be presented, that I have signed this document as my own free act and that all of the foregoing is true and correct.

IN TESTIMONY WHEREOF, I have hereunto set my hand this _____ day of _____, 2004

_____
Timothy L. Blankenship

STATE OF _____)
)ss.
COUNTY OF _____)

On this _____ day of _____, 2004, before me personally appeared Timothy L. Blankenship to me known and known to me to be the person described in and who executed the foregoing instrument, and he duly acknowledged to me that he executed the same for the uses and purposes therein set forth.

[SEAL]

_____
Notary Public

IN TESTIMONY WHEREOF, I have hereunto set my hand this _____ day of _____, 2004

_____
Sijian Chen

STATE OF _____)
)ss.
COUNTY OF _____)

On this _____ day of _____, 2004, before me personally appeared Sijian Chen to me known and known to me to be the person described in and who executed the foregoing instrument, and he duly acknowledged to me that he executed the same for the uses and purposes therein set forth.

[SEAL]

_____
Notary Public

244

300

FedEx Express *USA Airbill*

FedEx Tracking Number 8430 9018 1867

SAC11

Form I.D.No. 0215 **Sender's Copy**

1 From *Please print and press hard.*

Date

Sender's FedEx Account Number 2769-2324-2

Sender's Name SIJIAN CHEN Phone (206) 262-8900

Company DARBY & DARBY PC

Address 1191 2ND AVE STE 1900

Dept./Floor/Suite/Room

City SEATTLE State WA ZIP 98101-2993

2 Your Internal Billing Reference First 24 characters will appear on invoice. 08211/02000253-USO

3 To

Recipient's Name MATHEW GAFFNEY, ESQ. Phone ( )

Company DARBY & DARBY PC

Address 1191 SECOND AVE., STE. 1900

To "HOLD" at FedEx location, print FedEx address. We cannot deliver to P.O. boxes or P.O. ZIP codes.

Address

Dept./Floor/Suite/Room

City SEATTLE State WA ZIP 98101

4a Express Package Service *Packages up to 150 lbs.* Delivery commitment may be later in some areas.

- [X] FedEx Priority Overnight — Next business morning
- [ ] FedEx Standard Overnight — Next business afternoon
- [ ] FedEx First Overnight — Earliest next business morning delivery to select locations
- [ ] FedEx 2Day — Second business day
- [ ] FedEx Express Saver — Third business day

FedEx Envelope rate not available. Minimum charge: One-pound rate

4b Express Freight Service *Packages over 150 lbs.* Delivery commitment may be later in some areas.

- [ ] FedEx 1Day Freight* — Next business day
- [ ] FedEx 2Day Freight — Second business day
- [ ] FedEx 3Day Freight — Third business day

* Call for Confirmation:

5 Packaging * Declared value limit $500

- [X] FedEx Envelope*
- [ ] FedEx Pak* — Includes FedEx Small Pak, FedEx Large Pak, and FedEx Sturdy Pak
- [ ] Other

6 Special Handling Include FedEx address in Section 3.

- [ ] SATURDAY Delivery Available ONLY for FedEx Priority Overnight and FedEx 2Day to select ZIP codes
- [ ] HOLD Weekday at FedEx Location NOT Available for FedEx First Overnight
- [ ] HOLD Saturday at FedEx Location Available ONLY for FedEx Priority Overnight and FedEx 2Day to select locations

Does this shipment contain dangerous goods? One box must be checked.

- [ ] No
- [ ] Yes — As per attached Shipper's Declaration
- [ ] Yes — Shipper's Declaration not required
- [ ] Dry Ice — Dry Ice, 9, UN 1845 ____ x ____ kg

Dangerous Goods (including Dry Ice) cannot be shipped in FedEx packaging.

- [ ] Cargo Aircraft Only

7 Payment *Bill to:* Enter FedEx Acct. No. or Credit Card No. below.

- [ ] Sender — Acct. No. in Section 1 will be billed.
- [X] Recipient
- [ ] Third Party
- [ ] Credit Card
- [ ] Cash/Check

FedEx Acct. No. / Credit Card No. Exp. Date

Total Packages	Total Weight	Total Declared Value†	FedEx Use Only
1		$ .00	

†Our liability is limited to $100 unless you declare a higher value. See back for details.

8 Release Signature *Sign to authorize delivery without obtaining signature.*

By signing you authorize us to deliver this shipment without obtaining a signature and agree to indemnify and hold us harmless from any resulting claims.

447

NO POUCH NEEDED.
See back for peel and stick application instructions.

PULL AND RETAIN THIS COPY BEFORE AFFIXING TO THE PACKAGE.

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0260202970

SRF•Rev. Date 5/03•Part #157610•©1994–2003 FedEx•PRINTED IN U.S.A.

21APR 09:19 Empl# 52050 RTE#: 08

Recpt Addr: 9114 B SEDGEMOOR TR INCRT STR NAME/#

Pkg Trk#: 843090181856

Recip not at this Address

FedEx. PRIORITY OVERNIGHT WED

emp: 416339 20APR04

TRK# 8430 9018 1856 FORM 0215

Deliver By: 21APR04 A2

78748 2769232 42 AUS -TX-US XH AUSA

FedEx Urgent Express

Name Called shipper, left msg 04/21/04

Company

Address

City, State, Zip

Telephone

NO POUCH NEEDED.

See back for peel and stick application instructions.

RECIPIENT: PEEL HERE

FedEx USA Airbill Express

FedEx Tracking Number 8430 9018 1856

1 From This portion can be removed for Recipient's records.

Date 4-20-04 FedEx Tracking Number 843090181856

Sender's Name MATTHEW GAFFNEY, ESQ Phone 206 262-8900

Company DARBY & DARBY PC

Address 1191 2ND AVE STE 1900 Dept/Floor/Suite/Room

City SEATTLE State WA ZIP 98101-2993

2 Your Internal Billing Reference 08211/0200253-USO

3 To Recipient's Name Sijian Chen Phone

Company

Address 9114-B Sedgemoor Tr. We cannot deliver to P.O. boxes or P.O. ZIP codes.

To "HOLD" at FedEx location, print FedEx address. Dept/Floor/Suite/Room

Address

City Austin State TX ZIP 78748

8430 9018 1856

0260202970

Form ID No. 0215

4a Express Package Service — Packages up to 150 lbs. Delivery commitment may be later in some areas.

- [X] FedEx Priority Overnight — Next business morning
- [ ] FedEx Standard Overnight — Next business afternoon
- [ ] FedEx First Overnight — Earliest next business morning delivery to select locations
- [ ] FedEx 2Day — Second business day
- [ ] FedEx Express Saver — Third business day

FedEx Envelope rate not available. Minimum charge: One-pound rate

4b Express Freight Service — Packages over 150 lbs. Delivery commitment may be later in some areas.

- [ ] FedEx 1Day Freight* — Next business day
- [ ] FedEx 2Day Freight — Second business day
- [ ] FedEx 3Day Freight — Third business day

* Call for Confirmation: * Declared value limit $500

5 Packaging

- [X] FedEx Envelope*
- [ ] FedEx Pak* — Includes FedEx Small Pak, FedEx Large Pak, and FedEx Sturdy Pak
- [ ] Other

6 Special Handling — Include FedEx address in Section 3.

- [ ] SATURDAY Delivery — Available only for FedEx Priority Overnight and FedEx 2Day to select ZIP codes
- [ ] HOLD Weekday at FedEx Location — Not available for FedEx First Overnight
- [ ] HOLD Saturday at FedEx Location — Available only for FedEx Priority Overnight and FedEx 2Day to select locations

Does this shipment contain dangerous goods? One box must be checked.

- [ ] No
- [ ] Yes — As per attached Shipper's Declaration
- [ ] Yes — Shipper's Declaration not required
- [ ] Dry Ice — Dry Ice, 9, UN 1845 ____ x ____ kg
- [ ] Cargo Aircraft Only

Dangerous Goods (including Dry Ice) cannot be shipped in FedEx packaging.

7 Payment Bill to: Enter FedEx Acct. No. or Credit Card No. below. Obtain Recip. Acct. No. [ ]

- [X] Sender — Acct. No. in Section 1 will be billed.
- [ ] Recipient
- [ ] Third Party
- [ ] Credit Card
- [ ] Cash/Check

Total Packages 1 Total Weight Total Charges Credit Card Auth.

†Our liability is limited to $100 unless you declare a higher value. See the *FedEx Service Guide* for details.

8 Release Signature Sign to authorize delivery without obtaining signature.

By signing you authorize us to deliver this shipment without obtaining a signature and agree to indemnify and hold us harmless from any resulting claims.

Questions? Visit our Web site at fedex.com or call 1.800.Go.FedEx® 800.463.3339.

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447

PRINTED ON POST CONSUMER CONTENT

Livingston, Shannon

From: Gaffney Matthew
Sent: Wednesday, April 21, 2004 2:39 PM
To: Livingston, Shannon
Subject: FW: Message from an unidentified caller

Call from Fed. Ex—Sijian is no longer at the address we sent to him. See if you can find out what his current address is.

-----Original Message-----
From: Unity Messaging System - UNPRISEA
Sent: Wednesday, April 21, 2004 2:32 PM
To: Gaffney Matthew
Subject: Message from an unidentified caller

VoiceMessage (359 KB)

Livingston, Shannon

From: Gaffney Matthew
Sent: Sunday, April 25, 2004 2:04 PM
To: 'Sijian Chen'
Cc: Livingston, Shannon
Subject: RE: Formal papers for 08211/0200253-US0

Sijian,

Please sign and return the papers, or indicate that you refuse to sign them. Our deadline is Tuesday, April 27, 2004. Thank you in advance for you assistance.

Regards,
~Matt

-----Original Message-----
From: Gaffney Matthew
Sent: Monday, March 29, 2004 11:18 AM
To: 'Sijian Chen'
Cc: Livingston, Shannon
Subject: RE: Formal papers for 08211/0200253-US0

Sijian,

I understand that you may be reluctant to help National under the circumstances, and have other obligations that have higher priority.

We need to have either your signature on the declaration and the assignment, or proof that you refuse to execute these documents. If you are willing to sign these documents, please do so. If you refuse to do so, I would greatly appreciate it if you would mail us a letter stating that you refuse to execute the declaration and the assignment for Patent Application 10/724,028, filed on November 26, 2003, entitled "APPARATUS FOR CIRCUIT WITH KEEPER". Please mail the signed documents, or a letter stating your refusal, to Matthew Gaffney at Darby & Darby P.C., 1191 Second Avenue, Suite 1900, Seattle, Washington 98101.

Regards,
Matt

-----Original Message-----
From: Sijian Chen [mailto:schen4@austin.rr.com]
Sent: Sunday, March 28, 2004 2:31 PM
To: Gaffney Matthew
Cc: Livingston, Shannon
Subject: Re: Formal papers for 08211/0200253-US0

Matthew, Shannon,

I was let go by National at a difficult time of my life when I just had a new child and my wife was still sick at home. As much as I'd like to help National out completing the patent applications, I have many other obligations that's at higher priority. I'm afraid I do not have any time at the present to review the papers. Please remove my e-mail address and contact information from your contact list.

Rgs,

Sijian

----- Original Message -----
From: Gaffney Matthew
To: Schen4@austin.rr.com
Cc: Livingston, Shannon
Sent: Friday, March 26, 2004 2:09 PM
Subject: Formal papers for 08211/0200253-US0

Hello Sijian,

We previously sent you formal papers for your signature for the "keeper transistor" patent. Please let me know whether you are willing to sign these documents. Also, please let me know if there is anything we can do to make it more convenient for you to sign them and get them back to us. For you convenience, I am re-sending the formal papers to you.

<<Dec and POA.pdf>> <<Assignment.pdf>>

Attached please find: 1) a "corrected" Assignment and 2) a "corrected" Combined Declaration and Power of Attorney document. Please print the Assignment document (single-sided) and check that the information is correct. If the information is correct, please sign where indicated before a notary. Please print the Combined Declaration and Power of Attorney (single-sided) and also confirm the information is correct in this document. If the information is correct, please sign on the last page . Please return the signed documents by facsimile (fax number 206.262.8901) and by mail to Matthew Gaffney at Darby & Darby P.C., 1191 Second Avenue, Suite 1900, Seattle, Washington 98101. If there is incorrect information please let me know as soon as possible so we can correct the errors. We have a deadline of April 27, 2004 for filing these documents for "Missing Parts".

Should you have any questions, please do not hesitate to contact me.

Matthew M. Gaffney

Darby & Darby P.C.

1191 Second Avenue

Seattle, WA 98101

206.262.8910 | direct

206.262.8901 | fax

http://www.darbylaw.com

DARBY & DARBY
PROFESSIONAL CORPORATION

INTELLECTUAL PROPERTY LAW

SEATTLE
1191 SECOND AVENUE
SEATTLE, WA 98101
TEL 206.262.8900
FAX 206.262.8901

NEW YORK
805 THIRD AVENUE
NEW YORK, NY 10022-7513
TEL 212.527.7700
FAX 212.753.6237

, 2004

MATTHEW M. GAFFNEY
ATTORNEY AT LAW
206.262.8910
mgaffney@darbylaw.com

Reference: 08211/0200253-US0

VIA FEDERAL EXPRESS

Sijian Chen
12504 Edward Hollow Run
Austin, TX 78739

Re: **URGENT - Formal Papers for execution and return**

Dear Mr. Chen:

Enclosed please find a copy of the Application and Drawings as filed for the above-identified matter, for which you are a named inventor. Also enclosed is a copy of a notice received from the U.S. Patent and Trademark Office (USPTO) indicating that certain items are missing from the application as filed. The due date for filing these items was April 26, 2004 (we now are into the extension period).

We are also enclosing a Combined Declaration and Power of Attorney and an Assignment of this application for execution by you. If minor changes need to be made to correct for, *e.g.*, typographical errors, they can be made in pen. However, all such changes must be ***initialed and dated.***

Please return the executed documents to us (in the pre-paid Federal Express envelope) for filing with the USPTO as soon as you possibly can. If you have any questions or comments, please do not hesitate to contact me.

Very truly yours,

Matthew M. Gaffney

MMG/sml

Enclosures

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is described and claimed and for which a patent is sought on the invention entitled:

APPARATUS FOR CIRCUIT WITH KEEPER

the specification of which was filed on November 26, 2003 as Application No. 10/724,028.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to herein. I do not know and do not believe that the same was ever known or used in the United States of America before my or our invention thereof or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, or in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigned more than twelve months prior to this application.

I acknowledge the duty to disclose all information known to me that is material to patentability in accordance with Title 37, Code of Federal Regulations, § 1.56.

FOREIGN PRIORITY CLAIM

I hereby claim foreign priority benefits under Title 35, United States Code § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

[x] no such foreign applications have been filed

[ ] such foreign application have been filed as follows:

EARLIEST FOREIGN APPLICATION(S), IF ANY FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION

Application Number	Country	Date of Filing	Priority Claimed Under 35 USC 119
			___ Yes No ___

ALL FOREIGN APPLICATION(S), IF ANY FILED MORE THAN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION

Application Number	Country	Date of Filing

CLAIM FOR BENEFIT OF EARLIER U.S. PROVISIONAL APPLICATIONS

I hereby claim priority benefits under Title 35, United States Code §119(e), of any United States provisional patent application(s) listed below:

[x] no such U.S. provisional applications have been filed.

[ ] such U.S. provisional application have been filed as follows:

Application Number	Date of Filing	Priority Claimed Under 35 USC 119
		___ Yes No ___

CLAIM FOR BENEFIT OF EARLIER U.S./PCT APPLICATION(S)

I hereby claim the benefit under Title 35, United States Code, §120 of the United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose all information that is material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56 which became available to me between the filing date of the prior application and the national or PCT international filing date of this application:

[x] no such U.S./PCT applications have been filed.

[ ] such U.S./PCT application have been filed as follows:

Application Number	Date of Filing	Status (Patented/Pending/Abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made

with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the practitioners under Customer Number

38845

all of **Darby & Darby P.C.**, P.O. Box 5257, New York, New York 10150-5257, jointly, and each of them severally, my attorneys at law/patent agent(s), with full power of substitution, delegation and revocation, to prosecute this application, to make alterations and amendments therein, to receive the patent, and to transact all business in the U. S. Patent and Trademark Office connected therewith.

Please mail all correspondence to John W. Branch, whose address is:

Darby & Darby P.C.
P.O. Box 5257
New York, New York 10150-5257

Please direct telephone calls to: John W. Branch at (206) 262-8900.

Please direct facsimiles to: (212) 753-6237

Full name of sole or first inventor Timothy L. Blankenship	
Sole or first inventor's signature	Date
Residence Austin, Texas	
Citizenship US	
Mailing Address 4613 Saloma Place Austin, Texas 78749	

Full name of second inventor, if any Sijian Chen	
Second inventor's signature	Date
Residence Austin, Texas	
Citizenship China	
Mailing Address 9114-B Sedgemoor Tr. Austin, Texas 78748	

APPARATUS FOR CIRCUIT WITH KEEPER

Field of the Invention

The invention related to a keeper circuit. In particular, the invention related to a keeper circuit for ensuring that the high-range and low-range outputs of a circuit utilizing voltage doubling techniques are actively driven.

Background

Voltage doubling is a technique that makes it possible to design electrical circuits that operate with high power supply voltages (e.g. 10V or above), while not allowing the Vgs, Vgd, or Vds of the individual transistors in the circuit to exceed a lower value, such as 5V. The voltage doubling technique is often implemented with cascode transistors. In general, voltage doubling techniques may be used to extend the operating range to approximately 2X volts, where the underlying components can withstand X volts.

Brief Description of the Drawings

Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following drawings, in which:

Figure 1 illustrates a schematic diagram of a circuit that includes a keeper switch;

Figure 2 shows a schematic diagram of an exemplary embodiment of the circuit of Figure 1;

Figure 3 illustrates a schematic diagram of an exemplary embodiment of an inverter circuit with a keeper switch;

Figure 4 shows a schematic diagram of another exemplary embodiment of an inverter circuit with a keeper switch;

Figure 5 illustrates a schematic diagram of an exemplary embodiment of a level translator circuit with a keeper switch;

Figure 6 shows a schematic diagram of another exemplary embodiment of a level translator circuit with a keeper switch; and

Figure 7 illustrates a schematic diagram of another exemplary embodiment of a level translator circuit with a keeper switch, arranged in accordance with aspects of the present invention.

Detailed Description

Various embodiments of the present invention will be described in detail with reference to the drawings, where like reference numerals represent like parts and assemblies throughout the several views. Reference to various embodiments does not limit the scope of the invention, which is limited only by the scope of the claims attached hereto. Additionally, any examples set forth in this specification are not intended to be limiting and merely set forth some of the many possible embodiments for the claimed invention.

Throughout the specification and claims, the following terms take at least the meanings explicitly associated herein, unless the context clearly dictates otherwise. The meanings identified below are not intended to limit the terms, but merely provide illustrative examples for the terms. The meaning of "a," "an," and "the" includes plural reference, the meaning of "in" includes "in" and "on." The term "connected" means a direct electrical connection between the items connected, without any intermediate devices. The term "coupled" means either a direct electrical connection between the items connected, or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means either a single component or a multiplicity of components, either active and/or passive, that are coupled together to provide a desired function. The term "signal" means at least one current, voltage, charge, temperature, data, or other signal.

Briefly stated, the invention is related to a circuit with a keeper switch that is configured to minimize capacitive coupling between the gate and drain of a transistor arranged in a cascode configuration. The keeper switch is coupled between the source and gate of the cascode transistor. The keeper switch is active if a voltage at the drain of the keeper switch circuit corresponds to a first logic level. If this event occurs, the source and gate of the cascode transistor are coupled together.

Figure 1 illustrates a block diagram of a circuit (100) that includes a keeper switch circuit. Circuit 100 includes a first transistor (M0) and a second transistor (M1) configured in a cascode arrangement (104), and a keeper switch circuit (102). The second transistor (M1) has a gate that is coupled to a bias node (N12), a drain that is coupled to a first output node (N1), and a source that is coupled to a second output node (N2). The keeper switch circuit (102) has three terminals that are respectively coupled to the gate of the second transistor (M1), the drain of second transistor (M1), and the source of the second transistor (M1). The second transistor (M1) is configured to receive a first cascode bias voltage (bias) at the bias node (N12). The first cascode bias voltage (signal bias) is suitable as a cascode bias voltage.

The keeper switch circuit (102) is configured to influence a resistance between the second output node (N2) and the bias node (N12) in response to a control signal (e.g. signal bias). The keeper switch circuit (102) is configured to couple the second output node (N2) to the bias node (N12) if the control signal corresponds to a first logic level. The keeper switch circuit (102) is further configured to isolate the second output node (N2) from the bias node (N12) if the control signal corresponds to a second logic level.

In Figure 2, circuit 200 is a particular implementation of circuit 100, where the keeper switch circuit (102) is implemented by a transistor (M8). Transistor M8 has a gate that is coupled to the first output node (N1), a source that is coupled to the second output node (N2), and a drain that is coupled to the bias node (N12). Alternatively, the drain may be coupled to the second output node (N2), and the source may be coupled to the bias node (N12).

Figure 3 illustrates a schematic diagram of a circuit (300) that is an exemplary implementation of circuit 100. Circuit 300 is a high-voltage inverter that utilizes voltage doubling techniques. Circuit 300 includes transistors M2-M3 and M6-M7, and keeper switch circuit 102. Keeper switch circuit 102 is implemented by transistor M8. Transistor M8 has a gate that is coupled to node N1, a source that is coupled to node N2, and a drain that is coupled to node N11.

Transistors M2 and M3 are each arranged to operate as a cascode transistor. Transistor M2 is configured to receive a first bias signal Vsp at a gate of transistor M2 (node N11), and transistor M3 is configured to receive a second bias signal Vsn at a gate

of transistor M3 (node N13). Signal Vsp is a cascode bias voltage that is used to bias transistor M2, and signal Vsn is a cascode bias voltage that is used to bias transistor M3. The voltages associated with signals Vsp and Vsn are set by several factors including the power supply voltage, the maximum Vgs, Vgd, and Vds of the process for relatively long-term reliability, the threshold voltages of the transistors, the junction diode breakdowns of the transistors, and the input voltage swing. Signals Vsp and Vsn are selected such that the maximum Vgs, Vgd, and Vds of the transistors for relatively long-term reliability are not exceeded.

Transistor M6 is configured to receive a high-range signal in_hr at the gate of transistor M6, and transistor M7 is configured to receive a low-range signal in_lr at the gate of transistor M7. Signal in_lr is bounded between 0 volts and approximately Vdda/2, where Vdda is the voltage associated with the power supply. Signal in_hr is bounded between Vdda and approximately Vdda/2. Signal in_hr and signal in_lr each correspond to substantially the same logic level at approximately the same time. A high-range output signal (hr) is provided at the drain of transistor M6 (node N2). The logic level associated with signal hr corresponds to the inverse of the logic level of signals in_lr and in_hr. Circuit 300 is also configured to provide a full-range output signal (fr) at the source of transistor M2 (node N1), and a low-range output signal (lr) at the source of transistor M3 (node N3). Signals fr and lr each correspond to the same logic level as signal hr, but are bounded over different ranges. Signal lr is bounded between 0 volts and approximately Vdda/2, signal hr is bounded between approximately Vdda/2 and Vdda, and signal fr is bounded between 0 volts and Vdda.

Transistor M8 is configured to ensure that signal hr is actively driven regardless of the voltage associated with signals in_hr and in_lr, even at initial power-on. Transistor M8 is arranged for preventing charge injection (i.e. capacitive coupling) that could otherwise be caused as a result of the gate-to-drain capacitance on transistor M6. If present, injected charge could cause a voltage at the gate of transistor M6 to move outside of the desired operating range for Vgs, Vds, and Vgd of transistors M6. According to the example illustrated in Figure 3, transistor M2 is a p-type transistor, and transistor M8 is a p-type transistor.

Figure 4 illustrates a schematic diagram of a circuit (400) that is another exemplary implementation of Figure 1. Circuit 400 is substantially similar to circuit 300 in some ways, albeit different in other ways. In circuit 400, keeper switch circuit 102 is implemented by transistor M9. Transistor M9 has a gate that is coupled to node N1, a drain that is coupled to node N13, and a source that is coupled to node N3.

Transistor M9 is configured to ensure that signal lr is actively driven independent of the voltage associated with signals in_hr and in_lr, including at the initial power-on state. Transistors M3 and M9 are n-type transistors.

Figure 5 illustrates a schematic diagram of a level-shifter circuit (500). Circuit 500 includes transistors M2-M5 and M11-M16, keeper circuit 102 (transistor M8) and another keeper circuit (transistor M10). Transistor M4 has a gate that is coupled to node N11, a drain that is coupled to a first complement output node N21, and a source that is coupled to a second complement output node N22. Transistor M10 has a gate that is coupled to node N21, a source that is coupled to node N22, and a drain that is coupled to node N11.

Transistor M8 is configured to operate in a substantially similar manner as described with regard to Figure 3, albeit different in some ways. Transistor M4 is arranged to operate as a cascode transistor in cooperation with transistor M12. Transistor M5 is configured to operate as a cascode transistor in cooperation with transistor M14. Circuit 500 is configured to provide signals hr, fr, lr, hrb, frb, and lrb in response to a data input signal (din). Signal hrb is a complement of signal hr, signal frb is a complement of signal fr, and signal lrb is a complement of signal lr. As an example, transistors M2, M4, M8, and M10 are each p-type transistors. Transistor M8 is configured to ensure that signal hr is actively driven regardless of the voltage associated with signal din. Transistor M10 is configured to ensure that signal hrb is actively driven regardless of the voltage associated with signal din.

Figure 6 illustrates a schematic diagram of a circuit (600) that is substantially similar to circuit 500, albeit different in some ways. In this embodiment, the keeper circuit 102 is implemented by transistor M9, and the other keeper circuit is implemented by transistor M17. In this example, transistors M3, M5, M9, and M17 are n-type

transistors. Transistor M9 is configured to ensure that signal lr is actively driven. Transistor M17 is configured to ensure that signal lrb is actively driven.

Figure 7 illustrates a schematic diagram of a circuit (700) that is substantially similar to circuit 600, albeit different in some ways. In this embodiment, keeper circuit 102 is implemented by transistor M19, and the other keeper circuit is implemented by transistor M18. Keeper switch circuit 102 and the other keeper switch circuit are each coupled respectively to nodes N3, N13, and M23. Transistor M19 has a gate that is coupled to node N23, a source that is coupled to node N13, and a drain that is coupled to node N3. Transistor M18 has a gate that is coupled to node N3, a source that is coupled to node N13, and a drain that is coupled to node N23.

In this example, keeper switch circuit 102 is configured to influence a resistance between nodes N3 and M13. Keeper switch circuit 102 is configured to receive a control signal (e.g. signal lrb at node N23). Also, the keeper switch circuit 102 is further configured to couple node N3 to node N13 if the control signal corresponds to a first logic level (e.g. low). Additionally, keeper switch circuit 102 is further configured to isolate node N3 from node N13 if the control signal corresponds to a second logic level (e.g. high). In this example, transistors M3 and M5 are n-type transistors, and transistor M18 and M19 are p-type transistors.

The above specification, examples and data provide a description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention also resides in the claims hereinafter appended.

What is claimed is:

1. A circuit comprising:

a first transistor;

a second transistor that is arranged to operate as a cascode transistor in cooperation with the first transistor; and

a keeper switch circuit including three terminals that are respectively coupled to a gate, a drain, and a source of the second transistor.

2. The circuit of Claim 1, wherein

the second transistor is configured to receive a first cascode bias voltage at the gate of the second transistor, and wherein

the first cascode bias voltage is suitable for biasing a cascode transistor.

3. The circuit of Claim 1, wherein

the keeper switch circuit is configured to influence a resistance between the source and the gate of the second transistor in response to a control signal.

4. The circuit of Claim 1, wherein

the keeper switch circuit is configured to:

receive a control signal at the drain of the second transistor; and

couple the source of the second transistor to the gate of the second transistor if the control signal corresponds to a first logic level.

5. The circuit of Claim 4, wherein

the keeper switch circuit is further configured to isolate the source of the second transistor from the gate of the second transistor if the control signal corresponds to a second logic level.

6. The circuit of Claim 1, wherein

the keeper switch circuit comprises a keeper transistor including:

a gate that is coupled to the drain of the second transistor;

a source that is coupled to one of the source of the second transistor and the gate of the second transistor; and

a drain that is coupled to the other of the source of the second transistor and the gate of the second transistor.

7. The circuit of Claim 6, wherein

the second transistor is one of an n-type transistor and a p-type transistor, and the keeper transistor is the one of the n-type transistor and the p-type transistor.

8. The circuit of Claim 6, wherein

the second transistor is one of an n-type transistor and the p-type transistor, and the keeper transistor is the other of the n-type transistor and the p-type transistor.

9. The circuit of Claim 1, further comprising:

a third transistor;

a fourth transistor that is arranged to operate as a cascode transistor in cooperation with the third transistor; and

another keeper switch circuit including three terminals that are respectively coupled to a gate, a drain, and a source of the fourth transistor.

10. The circuit of Claim 9, wherein

the other keeper switch circuit comprises a fifth transistor including:

a gate that is coupled to the drain of the fourth transistor,

a source that is coupled to one of the source of the fourth transistor and the gate of the second transistor, and

a drain that is coupled to the other of the source of the fourth transistor and the gate of the second transistor.

11. A logic circuit comprising:

a first transistor;

a second transistor that is arranged to operate as a cascode transistor in cooperation with the first transistor, wherein the second transistor includes:

a gate that is coupled to a bias node,

a drain that is coupled to a first output node, and

a source that is coupled to a second output node;

a third transistor;

a fourth transistor that is arranged to operate as a cascode transistor in cooperation with the third transistor, wherein the fourth transistor includes:

a gate that is coupled to the bias node,

a drain that is coupled to a first complement output node, and

a source that is coupled to a second complement output node,

a first keeper switch circuit that is coupled to the bias node, the second complement output node, and the second output node, and

a second keeper switch circuit that is coupled to the bias node, second output node, and the second complement output node.

12. The logic circuit of Claim 11, wherein

the second transistor is configured to receive a first cascode bias voltage at the bias node, wherein

the first cascode bias voltage is suitable for biasing a cascode transistor.

13. The logic circuit of Claim 11, wherein

the first keeper switch circuit is configured to influence a resistance between the second output node and the bias node in response to a control signal.

14. The logic circuit of Claim 11, wherein

the first keeper switch circuit is configured to:

receive a control signal at the second complement output node;

couple the second output node to the bias node if the control signal corresponds to a first logic level; and

isolate the second output node from the bias node if the control signal corresponds to a second logic level.

15. The logic circuit of Claim 11, wherein

the logic circuit is arranged to operate as a level shifter circuit.

16. The logic circuit of Claim 11, wherein

the first keeper switch circuit comprises a keeper transistor including:

a gate that is coupled to the second complement output node,

a source that is coupled to one of the second output node and the bias node, and

a drain that is coupled to the other of the second output node and the bias node.

17. The logic circuit of Claim 16, wherein

the second transistor is one of an n-type transistor and a p-type transistor, and the keeper transistor is the other of the n-type transistor and the p-type transistor.

18. The logic circuit of Claim 11, wherein

the second keeper switch circuit comprises a fifth transistor including:

a gate that is coupled to the second output node,

a source that is coupled to one of the second complement output node and the bias node, and

a drain that is coupled to the other of the second complement output node and the bias node.

19. The logic circuit as in Claim 18, wherein

the first keeper switch circuit comprises a keeper transistor, and

wherein the second transistor is one of an n-type transistor and a p-type transistor, the keeper transistor is the other of the n-type transistor and the p-type transistor, and the fifth transistor is the other of the n-type transistor and the p-type transistor.

20. A circuit comprising:

a transistor that is configured as a cascode transistor; and

means for coupling a source of the transistor to a gate of the transistor if a voltage associated with a drain of the transistor corresponds to a first logic level.

Abstract

A keeper switch circuit is configured to minimize capacitive coupling between the gate and drain of a cascode transistor. The keeper switch circuit is coupled between the source and gate of a cascode transistor. The keeper switch circuit is on if a voltage at the drain of the keeper switch circuit corresponds to a first logic level. The source and gate of the cascode transistor are coupled together if the keeper switch circuit is on.

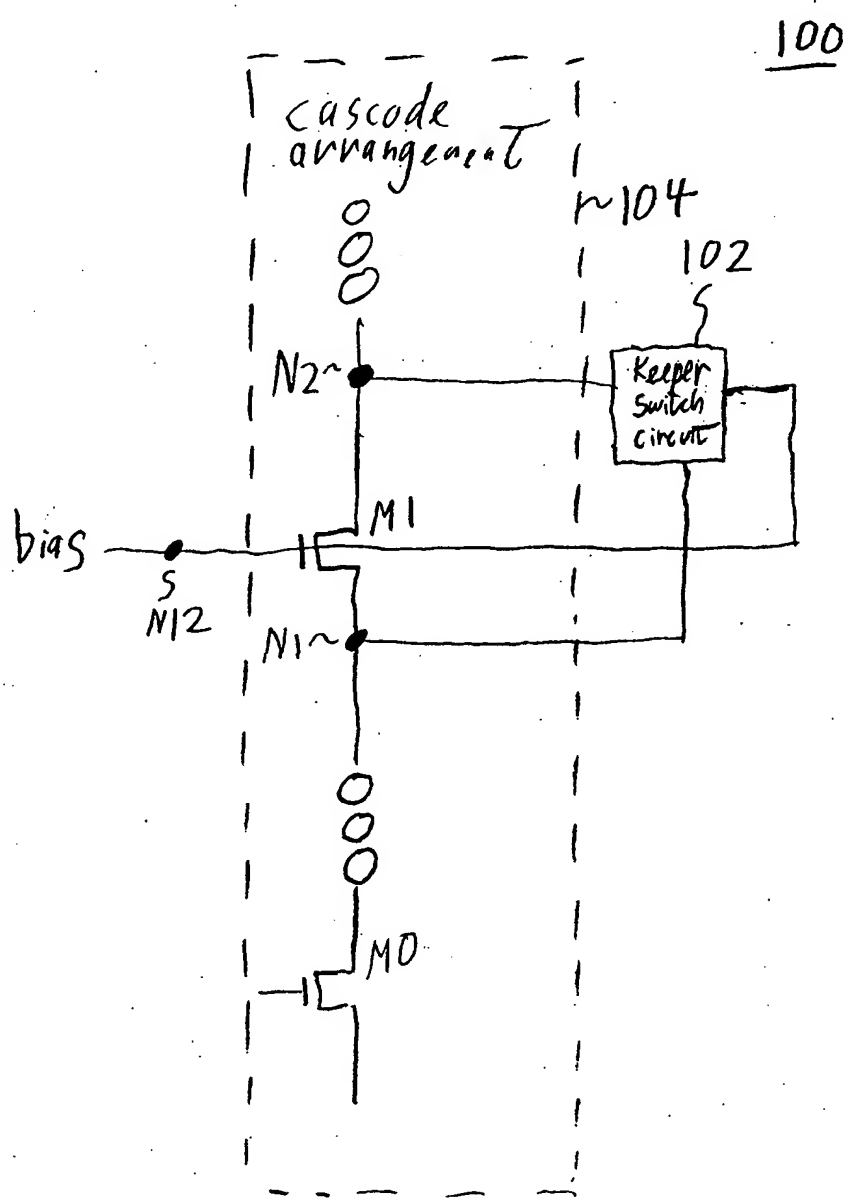

100
cascode arrangement
~104
102
N2~
Keeper Switch circuit
M1
bias
S
N12
N1~
M0

Figure 1

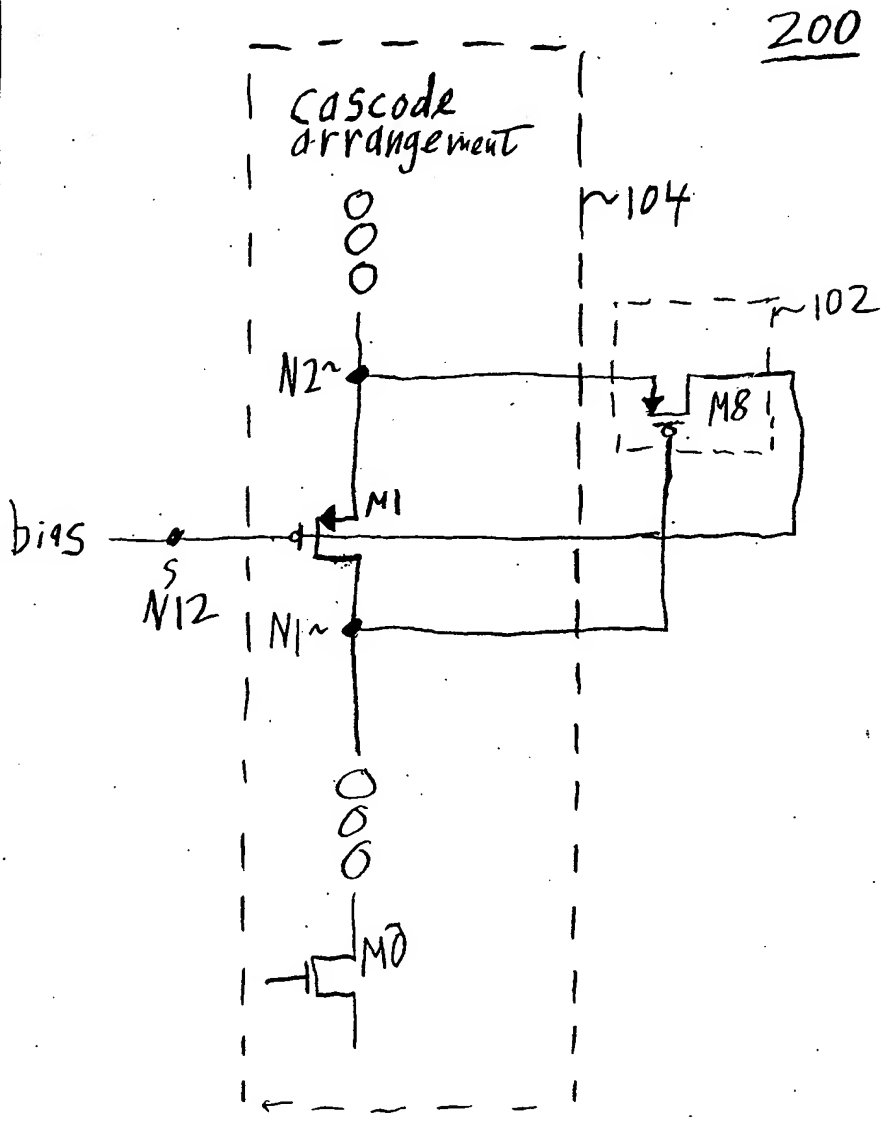
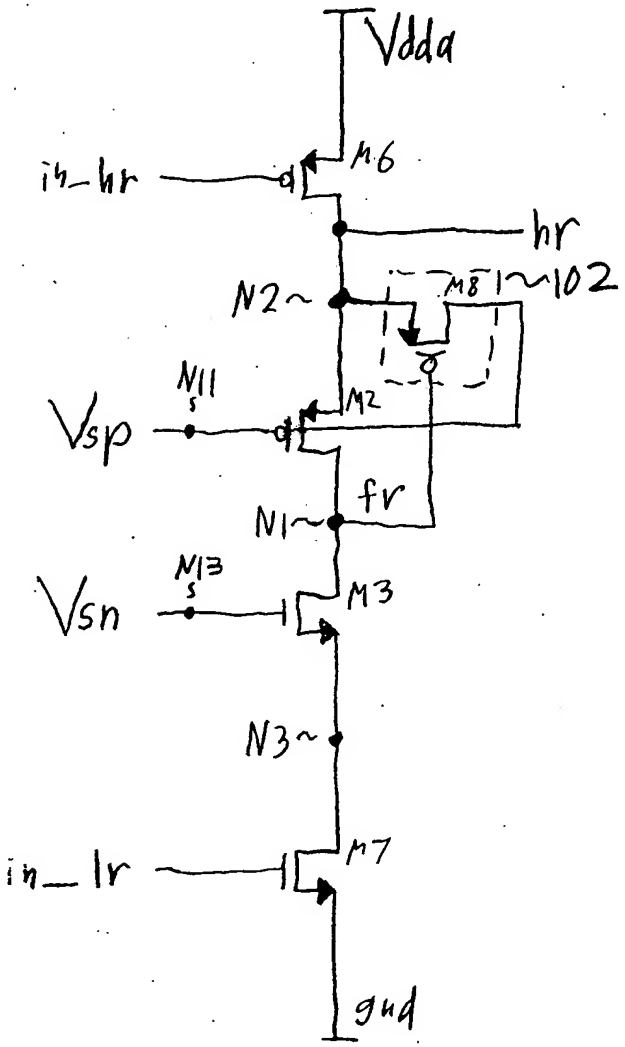


Figure 2

300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M6
hr
N2
M8
102
Nll
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M2
Vsp
fr
N1
Nl3
s
Vsn
M3
N3
in_lr
M7
gnd

Figure 3

400

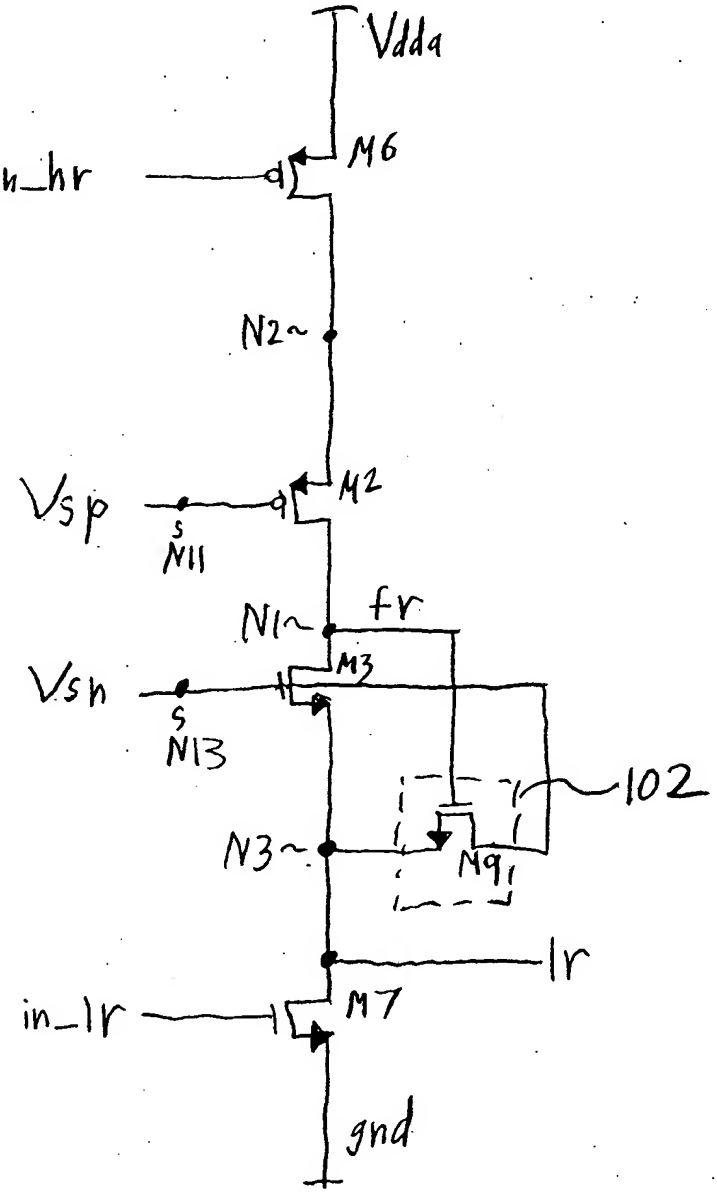


Figure 4

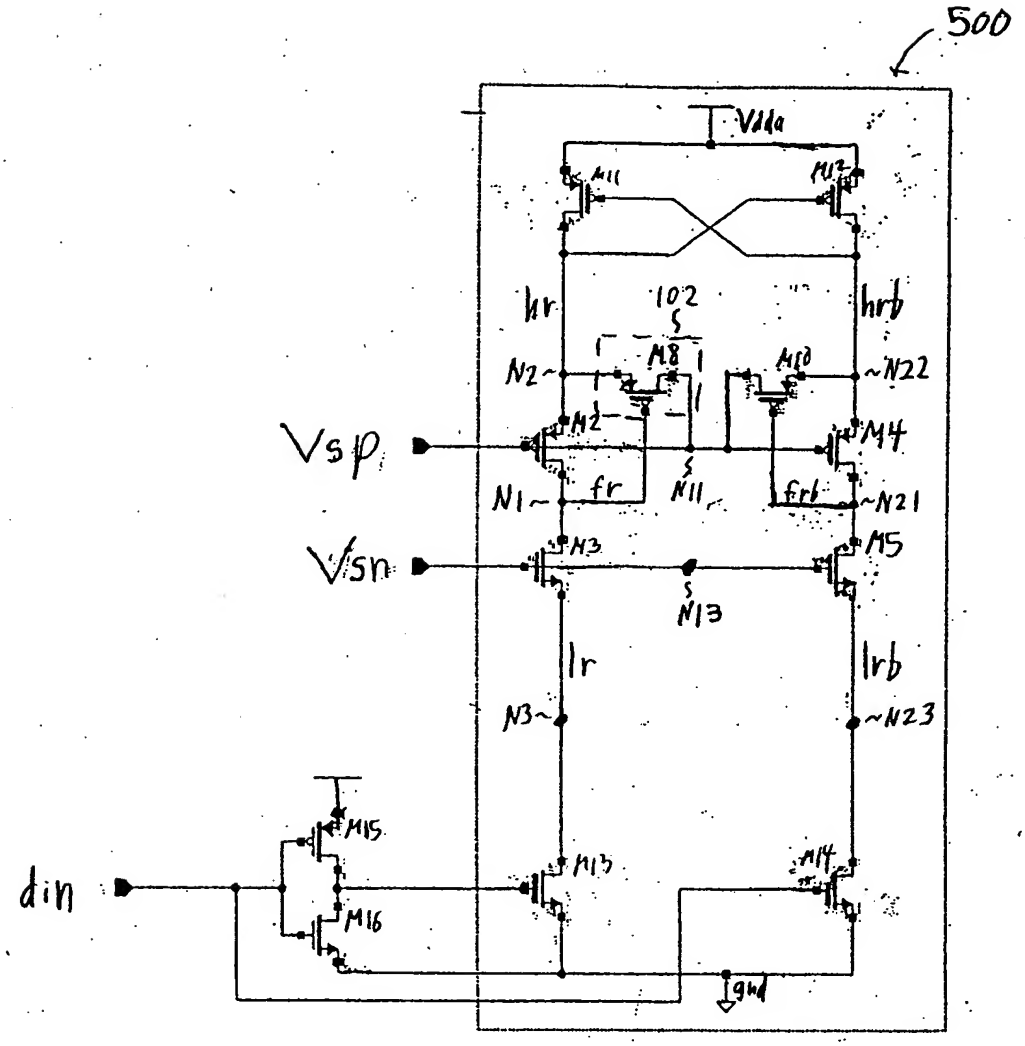
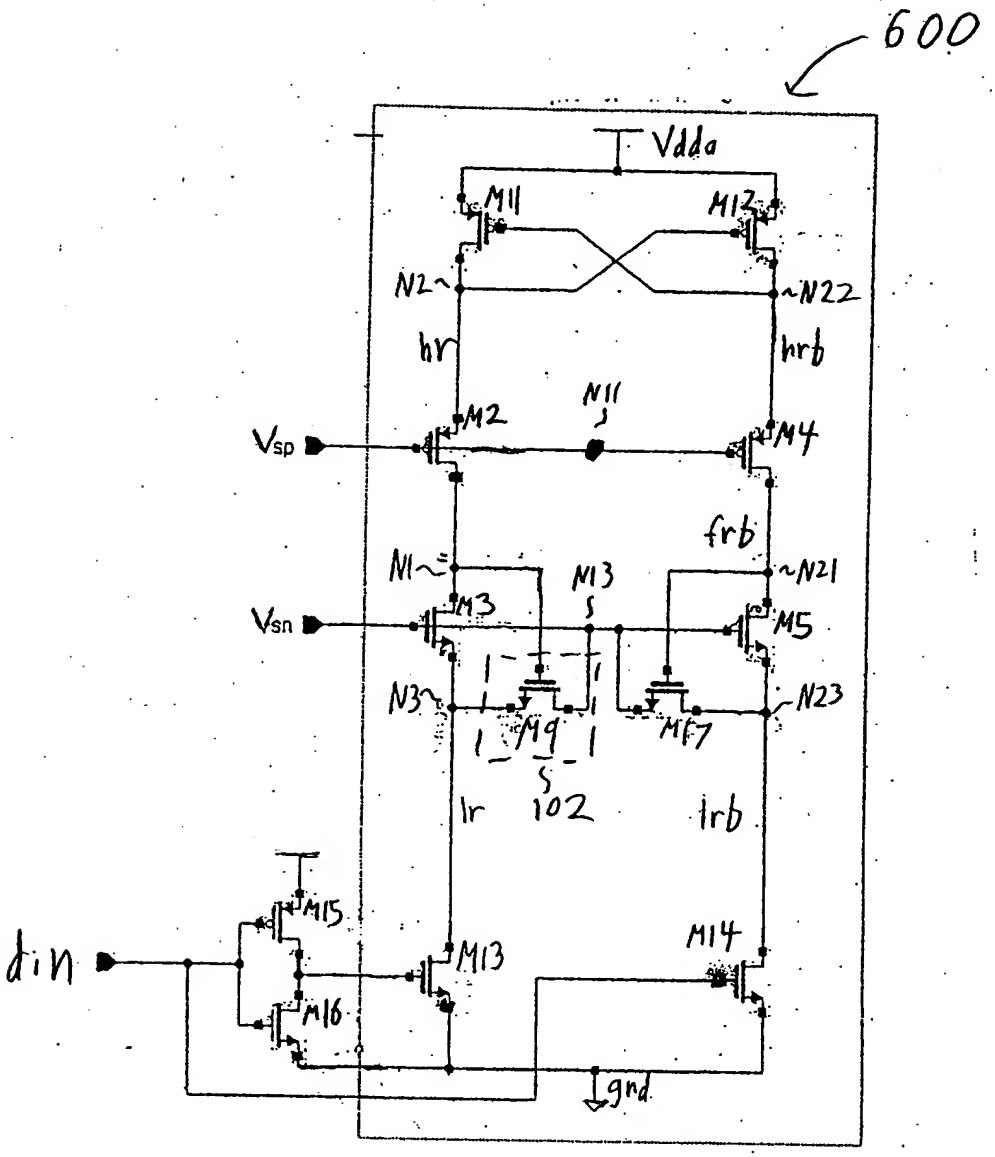

500
Vdda
M11
M12
hr
102
hrb
N2
M8
M10
N22
M2
M4
Vsp
N1
fr
N11
frb
N21
Vsn
N3
M5
N13
lr
lrb
N3
N23
M15
din
M16
M13
M14
gnd

Figure 5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Vdda
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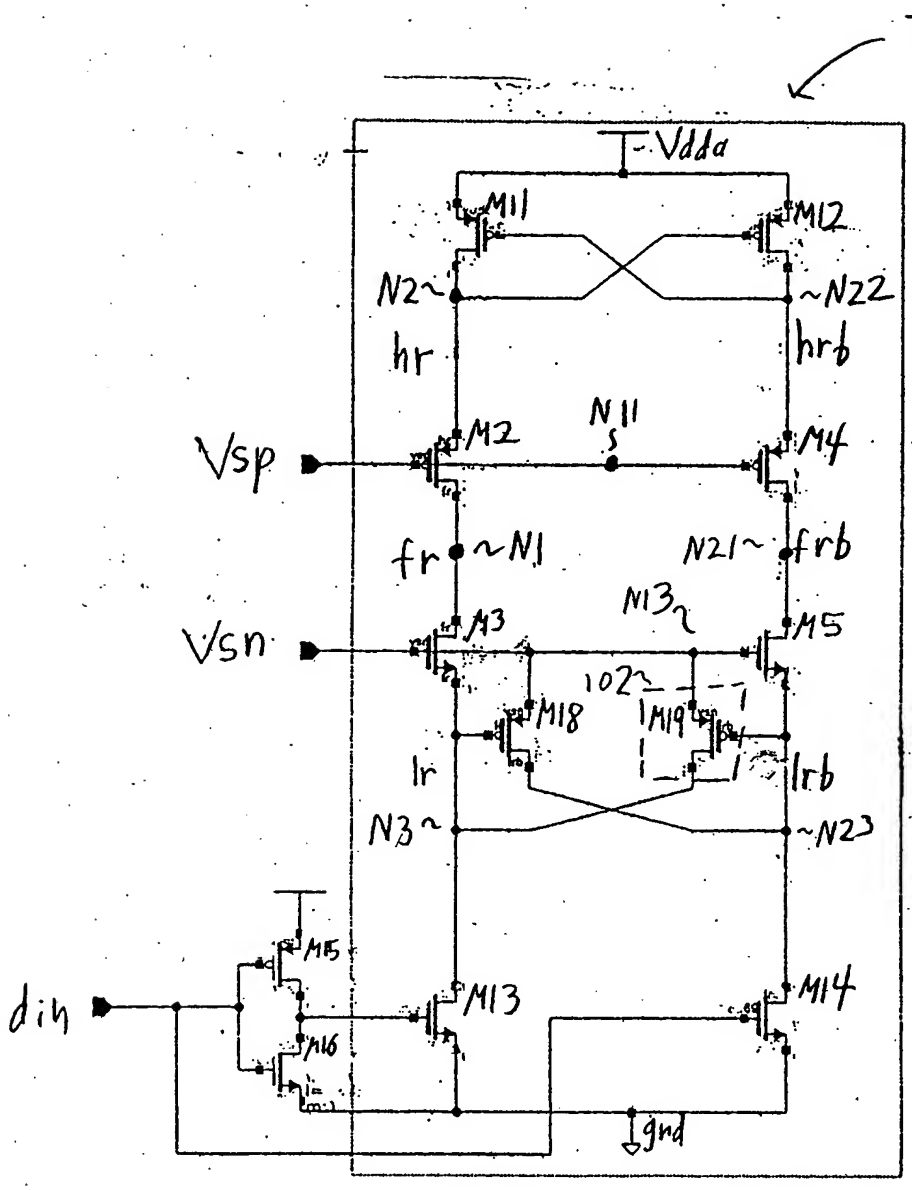
M12
N2
N22
hr
hrb
M2
N11
M4
Vsp
frb
N1
M13
N21
M3
M5
Vsn
N3
N23
M9
M7
lr
102
lrb
M15
M13
M14
din
M16
gnd

Figure 6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frb
Vsn
M3
N13
M5
102
M18
M19
lr
lrb
N3
N23
M15
M13
M14
din
M16
gnd

Figure 7

ASSIGNMENT

I, Timothy L. Blankenship, a citizen of US, residing at 4613 Saloma Place; Austin, Texas 78749; and

I, Sijian Chen, a citizen of China, residing at 9114-B Sedgemoor Tr.; Austin, Texas 78748;

and each of us, if more than one person is identified above (hereinafter "ASSIGNOR") in consideration of the sum of Ten Dollars ($10.00), or the equivalent thereof, and other good and valuable consideration, the sufficiency of which and receipt of which are hereby acknowledged, paid to ASSIGNOR by

National Semiconductor Corporation

a Corporation organized under the laws of Delaware, located at 2900 Semiconductor Drive, Santa Clara, California 95051-8090 (hereinafter "ASSIGNEE"), do hereby sell and assign to said ASSIGNEE, its successors and assigns, the below indicated right, title, and interest, **throughout the world** in and to my Invention entitled:

APPARATUS FOR CIRCUIT WITH KEEPER

invented by me and described in Patent Application No. 10/724,028, filed on November 26, 2003, in the United States; and all patents, divisions, reissues, continuations and any extensions thereof and rights of priority therein, said interest being my entire ownership interest in the same, to be held and enjoyed by said ASSIGNEE, its successors, assigns, or other legal representatives, to the full end of the term thereof, as fully and entirely as the same would have been held and enjoyed by me if this assignment and sale had not be made;

And for the consideration aforesaid, I hereby covenant and agree to and with said ASSIGNEE, its successors and assigns, that whenever ASSIGNEE, its counsel or representative, or the counsel or representative of its successors or assigns, shall advise that an amendment to, or

a division of, or any other proceeding or action in connection with an application concerning said Invention, including interference proceedings, is lawful and desirable, or that a reissue or continuation or extension of such application or patent issuing therefrom is lawful and desirable, I will sign all papers and drawings, take all rightful oaths and affidavits, and do all acts necessary or required to be done for the procurement of all lawful rights associated with the Invention, or for the reissue or continuation or extension of the same, will do all acts necessary or required to secure in said ASSIGNEE, its successors or assigns, the title to and full benefit of all rights hereby assigned, without charge to said ASSIGNEE or its successors or assigns, but at its or their expense; and I hereby appoint every present or future officer of said ASSIGNEE as my agent to sign all such papers and to do all such necessary acts on my behalf, to the fullest extent permitted by law;

And I hereby authorize and request the Commission of Patents and Trademarks and any other granting authority to issue any Letters Patent resulting from said Invention and application(s) concerning same to said ASSIGNEE.

This assignment shall have an effective date corresponding to the last date of execution.

I declare under penalty of perjury under the laws of the United States of America, and under penalty of the laws of any other jurisdiction before which this document may be presented, that I have signed this document as my own free act and that all of the foregoing is true and correct.

IN TESTIMONY WHEREOF, I have hereunto set my hand this _____ day of _____, 2004

_____
Timothy L. Blankenship

STATE OF _____)
)ss.
COUNTY OF _____)

On this _____ day of _____, 2004, before me personally appeared Timothy L. Blankenship to me known and known to me to be the person described in and who executed the foregoing instrument, and he duly acknowledged to me that he executed the same for the uses and purposes therein set forth.

[SEAL]

_____
Notary Public

IN TESTIMONY WHEREOF, I have hereunto set my hand this _____ day of _____, 2004

_____
Sijian Chen

STATE OF _____)
)ss.
COUNTY OF _____)

On this _____ day of _____, 2004, before me personally appeared Sijian Chen to me known and known to me to be the person described in and who executed the foregoing instrument, and he duly acknowledged to me that he executed the same for the uses and purposes therein set forth.

[SEAL]

_____
Notary Public

FedEx Express USA Airbill

8457 3654 2280

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FedEx Envelope rate not available. Minimum charge: One-pound rate

4b Express Freight Service — Packages over 15

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* Call for Confirmation:

5 Packaging * Declared value lir

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- ☐ FedEx Pak* — Includes FedEx Small Pak, FedEx Large Pak, and FedEx Sturdy Pak
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Total Packages	Total Weight	Total Declared Value†
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City SEATTLE State WA ZIP 98101-2993

2 Your Internal Billing Reference First 24 characters will appear on invoice. OPTIONAL

3 To

Recipient's Name Matthew Gaffney Phone (206) 262-8900

Company Darby & Darby PC

Address 1191 2nd Ave

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City Seattle State WA ZIP 9810[illegible]

4a Express Package Service — Packages up to 15

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- ☑ FedEx Standard Overnight — Next business afternoon
- ☐ FedEx First Overnight — Earliest next business morning delivery to select locations
- ☐ FedEx 2Day — Second business day
- ☐ FedEx Express Saver — Third business day

FedEx Envelope rate not available. Minimum charge: One-pound rate

4b Express Freight Service — Packages over 15

- ☐ FedEx 1Day Freight* — Next business day
- ☐ FedEx 2Day Freight — Second business day
- ☐ FedEx 3Day Freight — Third business day

* Call for Confirmation:

5 Packaging * Declared value lir

- ☑ FedEx Envelope*
- ☐ FedEx Pak* — Includes FedEx Small Pak, FedEx Large Pak, and FedEx Sturdy Pak
- ☐ Other

6 Special Handling — Include FedEx address in Section 3.

- ☐ SATURDAY Delivery — Available ONLY for FedEx Priority Overnight, FedEx 2Day, FedEx 1Day Freight, and FedEx 2Day Freight to select ZIP codes
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Dangerous Goods (including Dry Ice) cannot be shipped in FedEx packaging. ☐ Cargo Aircraft Only

7 Payment *Bill to:* Enter FedEx Acct. No. or Credit Card No. below.

- ☐ Sender — Acct. No. in Section 1 will be billed.
- ☑ Recipient
- ☐ Third Party
- ☐ Credit Card
- ☐ Cash/C

FedEx Acct. No. / Credit Card No. 2769-2324-2 Exp. Date

Total Packages	Total Weight	Total Declared Value†
1		$ 1 .00

†Our liability is limited to $100 unless you declare a higher value. See back for details. FedEx Use O

8 Release Signature *Sign to authorize delivery without obtaining signature.*

By signing you authorize us to deliver this shipment without obtaining a signature and agree to indemnify and hold us harmless from any resulting claims.

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By using this Airbill you agree to the service conditions on the back of this Airbill and in our current Service Guide, including terms that limit our liability.

Questions? Visit our Web site at fedex.com or call 1.800.Go.FedEx® 800.463.3339.

0275664639

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Track Shipments
Detailed Results

Printable Version Quick Help

Select another track: 845736542280 Next

Tracking number	845736542280	**Reference number**	0821110200253-USO
Ship date	Apr 27, 2004	**Delivery location**	AUSTIN TX
Estimated delivery reattempt date	Apr 29, 2004 by 4:30 pm	**Service type**	Standard Envelope

Date/time		Status	Location	Comments
Apr 28, 2004	10:33 am	**Delivery attempt**	AUSTIN TX	Customer not available or Business closed
	10:33 am	On FedEx vehicle for delivery	AUSTIN TX	
	7:52 am	On FedEx vehicle for delivery	AUSTIN TX	
	6:40 am	Arrived at FedEx Destination Location	AUSTIN TX	
	5:45 am	Left FedEx Ramp	AUSTIN TX	
	5:09 am	Arrived at FedEx Ramp	AUSTIN TX	
	4:28 am	Left FedEx Sort Facility	MEMPHIS TN	
	2:01 am	Left FedEx Sort Facility	MEMPHIS TN	
	1:18 am	Arrived at Sort Facility	MEMPHIS TN	
Apr 27, 2004	7:21 pm	Left FedEx Ramp	SEATTLE WA	
	6:43 pm	Arrived at FedEx Ramp	SEATTLE WA	
	4:43 pm	Picked up by FedEx	SEATTLE WA	
	3:33 pm	Left FedEx Origin Location	SEATTLE WA	

Signature proof | Track more shipments | << Track summary

Email your detailed tracking results (optional)

Enter your email, submit up to three email addresses (separated by commas), add your message (optional), and click **Send email**.

From
To

Add a message to this email.

Send email